# Short Range Communication System on Vehicular Application

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*Abstract* - **The dedicated short-range communication (DSRC) is a latest technology to push the intelligent transportation system into our day to day life and is very important architecture in VLSI. Dedicated Short Range Communication (DSRC) is a key enabling technology for the next generation communication-based safety applications. One motive of vehicular safety com-munication is the routine broadcast of messages among all equipped vehicles. The DSRC standards generally adopt FM0 and Manchester codes to reach dc-balance, which enhances the signal reliability. This paper depicts the various parts of the DSRC system and its application in VANITY application. Manchester encoder and FM0 encoder has been used as the encoding technique for the channel transmission. In this paper a vehicular DSRC system is prepared using the vehicular model. Vehicular systems administration can include vehicle-to-vehicle (V2V) correspondence, vehicle-to-framework (V2I) correspondence. This paper not only develops a Vehicular DSRC system VLSI , but also exhibits an efficient performance compared with the existing works.**

*Index terms*- **Dedicated short range communication (DSRC), Vehicular adhoc network (VANITY) , FM0, V2V , V2I .**

## I. INTRODUCTION

THE dedicated short-range communication (DSRC) [1] is a protocol for one- or two-way medium range communication especially for intelligent transportation systems. The DSRC can be briefly classified into two categories: automobile-to-automobile and automobile-to-roadside. In automobile-to-automobile, the DSRC enables the message sending and broadcasting among automobiles for safety issues and public information announcement . The safety issues include blind-spot, intersection warning, inter cars distance, and collision-alarm. The automobile-to-roadside focuses on the intelligent transportation service, such as electronic toll collection (ETC) system. With ETC, the toll collecting is electrically accomplished with the contactless IC-card platform. Moreover, the ETC can be extended to the payment for parking-service, and gas-refueling. Thus, the DSRC system plays an important role in modern automobile industry. The system architecture of DSRC transceiver is shown in Fig. 1. The upper and bottom parts are dedicated for transmission and receiving.

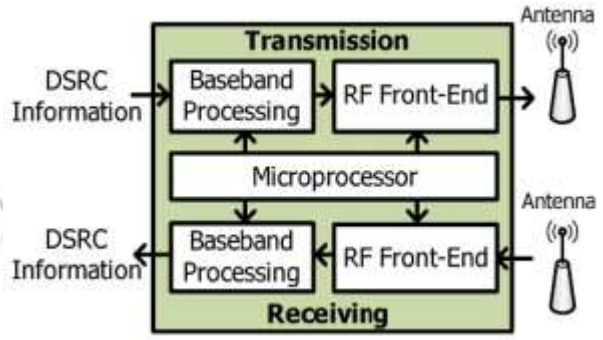


**Fig.1.Architecture of DSRC system.**

This transceiver is classified into three basic modules: microprocessor, baseband processing, and RF front-end. The microprocessor interprets instructions from media access control to schedule the tasks of baseband processing and RF front-end. The baseband processing is responsible for modulation, error correction, clock synchronization, and encoding. The RF frontend transmits and receives the wireless signal through the antenna. In 1999, the U.S. Federal Communication Commission allocated 75MHz of Dedicated Short Range Communication (DSRC) spectrum at 5.9GHz to be used exclusively for vehicle-to-vehicle and infrastructure-to-vehicle communications. The primary purpose is to enable public safety applications that save lives and improve traffic flow. Private services are also permitted in order to lower cost and to encourage DSRC development and adoption. These systems provide an extended information horizon to warn the driver or the vehicle systems of (po-tentially) dangerous situations in a much earlier phase.This paper provides an overview of the nature of vehicular safety communications. Devoted Short-Range Communications (DSRC) is 75 MHz of range at 5.9 GHz allocated by the Federal Communications Commission (FCC) to "increase traveller safety, reduce fuel consumption and pollution, and continue to advance the nation's economy. This promising development is designed to support vehicle to- vehicle and vehicle-to-infrastructure communication using a variant of the IEEE 802.1 a technology .

The purposes of FM0 and Manchester codes can provide the transmitted signal with dc-balance. Both FM0 and Manchester codes are widely adopted in encoding for downlink. The VLSI architectures The VLSI architectures of FM0 and Manchester encoders are reviewed as follows

## II. METHODOLOGY

### *MANCHESTER ENCODING*

The Manchester coding example is shown in Fig. 4. The Manchester code is derived from

$$X \oplus \text{CLK}. \qquad (1)$$

The Manchester encoding is realized with a XOR operation for CLK and *X*. The clock always has a transition within one cycle, and so does the Manchester code no matter what the *X* is.

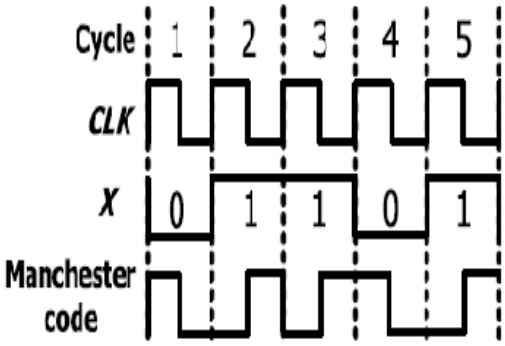


Fig.2. Waveform Of Manchester Encoder

In Manchester encoding the average power is always the same, no matter what data is transmitted. Compared to all other encoding methods, Manchester code follows an algorithm to encode the data. It always produces a transition at the center of the bit. It contains sufficient information to recover a clock. So if the data rate is twice, sufficient clock information can be recovered from the data stream so that separate clocks are not needed. As a result, the electrical connection using Manchester code is easily a galvanic ally isolator (it is the principle of isolating functional sections of electric systems to prevent current flow) using a network isolator for simple one-to-one isolation transformation. Therefore, while transmitting the data, the number of wires is minimized, which is used to reduce the noise and transmission power.

□□Logic “1” represents the transition from HIGH to LOW.

□□Logic “0” represents the transition from LOW to HIGH.

To acquire a fast, give a synchronized information source as the primary clock beat for information. While transmitting the information, it is an advanced encoding in which information transmission bits are spoken to by moves starting with one rationale then onto the next rational. The length of each bit is set as default, and it consumes the signals as self-clocking. The direction of the transition decides the state of the bit.

### *FM0 ENCODING*

The coding principle of FM0 is listed as the following three rules.

1) If *X* is the logic-0, the FM0 code must exhibit a transition between *A* and *B*.

2) If *X* is the logic-1, no transition is allowed between *A* and *B*.

3) The transition is allocated among each FM0 code no matter what the *X* is.

A FM0 coding example is shown in Fig. 3. At cycle 1, the *X* is logic-0; therefore, a transition occurs on its FM0 code, according to rule 1. For simplicity, this transition is initially set from logic-0 to -1. According to rule 3, a transition is allocated among each FM0 code, and thereby the logic-1 is changed to logic-0 in the beginning of cycle 2. Then, according to rule 2, this logic-level is hold without any transition in entire cycle 2 for the *X* of logic-1. Thus, the FM0 code of each cycle can be derived with these three rules mentioned earlier.

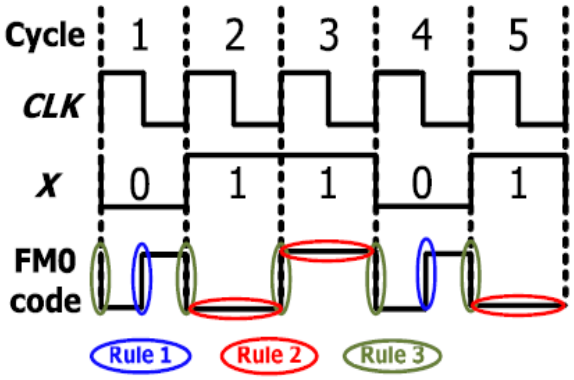


**Fig.3. Waveform of FM0 encoding**

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## III. HARDWARE ARCHITECTURE OF THE ENCODER

The encoder is developed using these two encoding techniques i.e, Manchester and fm0 encoding techniques and a multiplexer is put in the architecture for the selection of the encoder so as to which encoder is to be used. This is the equipment engineering of the fm0/Manchester code. the top part is meant the fm0 code and after that the base part is meant as the Manchester code. in fm0 code the D flip lemon are utilized to store the state code of the fm0 code furthermore multiplexer and not entryway is utilized as a part of the fm0 code. The delay time of Manchester encoding is smaller than that of FM0 encoding. Thus, the operation frequency of Manchester encoding is faster than that of the FM0 encoding. When the mode=0 is for the fm0 code The Manchester code is developed only using the XOR gate and when the mode=1 is for the Manchester code.

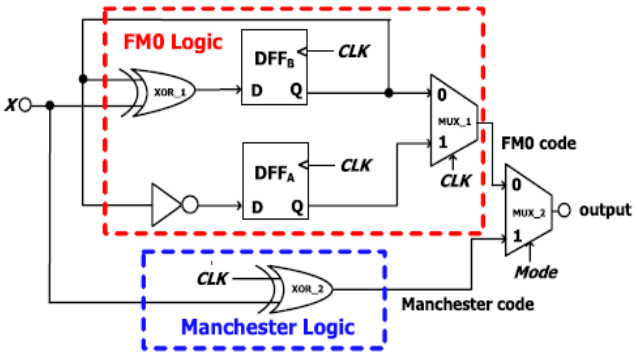


**Fig.4. Architecture of Encoder**

Now the encoder is developed for the channel encoding . The encoder consists of both the encodings Manchester and FM0 encoding connected to the multiplexer. A module selecter is applied to the architecture in which when the select line is 0 so Manchester encoder is active and when the module selecter is 1 then FM0 is active.

*Theory of operation*

Dedicated short range communication system have to be designed which consist of a transmitter and a receiver and a microprocessor .The microprocessor interprets instructions from media access control to schedule the tasks of baseband processing and RF front-end. The output will be obtained using the modelsim software. The dedicated short range communication system will be applied to the vehicular model and a vehicular dsrc system will be designed by using VHDL hardware language with considering timing constraints. The system architecture of DSRC transceiver is shown in Fig. 1. The upper and bottom parts are dedicated for transmission and receiving This transceiver is classified into three basic modules: microprocessor, baseband processing, and RF front-end. The microprocessor interprets instructions from media access control to schedule the tasks of baseband processing and RF front-end..

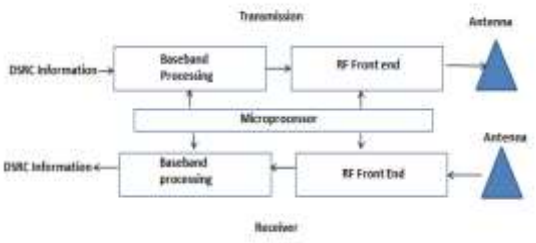


Fig.5. DSRC SYSTEM

This transceiver is classified into three basic modules: microprocessor, baseband processing, and RF front-end. The microprocessor interprets instructions from media access control to schedule the tasks of baseband processing and RF front-end.

The baseband processing is responsible for modulation, error correction, clock synchronization, and encoding. The RF front end transmits and receives the wireless signal through the antenna .

## (IV) VEHICULAR MODEL

In the vehicular model which we are using there are seventy two bits out of which sixty four bits are data message bits and eight bits are channel bits . four bits are used for the source channel and four bits are used for the destination channel . There are six service channels (SCH) and one control channel (CCH). The control channel is utilized for framework control and security information transmission. Then again, benefit channels are appointed for trade of non-security related information. Also, these channels use different frequencies and transmit powers. Multi-channel operation helps both types of communication simultaneously so that the problem of contention between applications can be avoided.

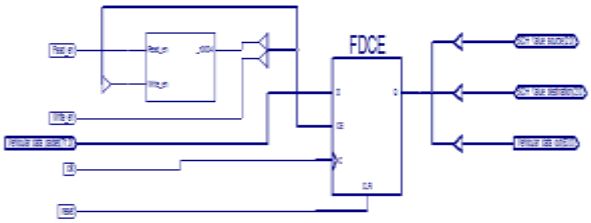


**Fig.6. Vehicular Model**

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## (V) VEHICULAR DSRC USING VEHICULAR MODEL

The dedicated short range communication system is applied to the vehicular model and a vehicular dsrc system is designed by using VHDL hardware language with considering timing constraints.

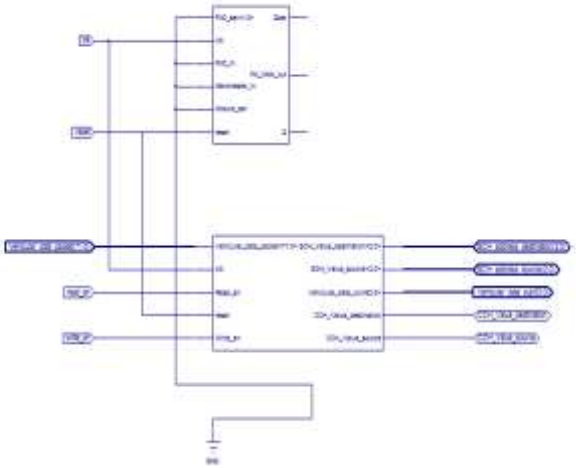
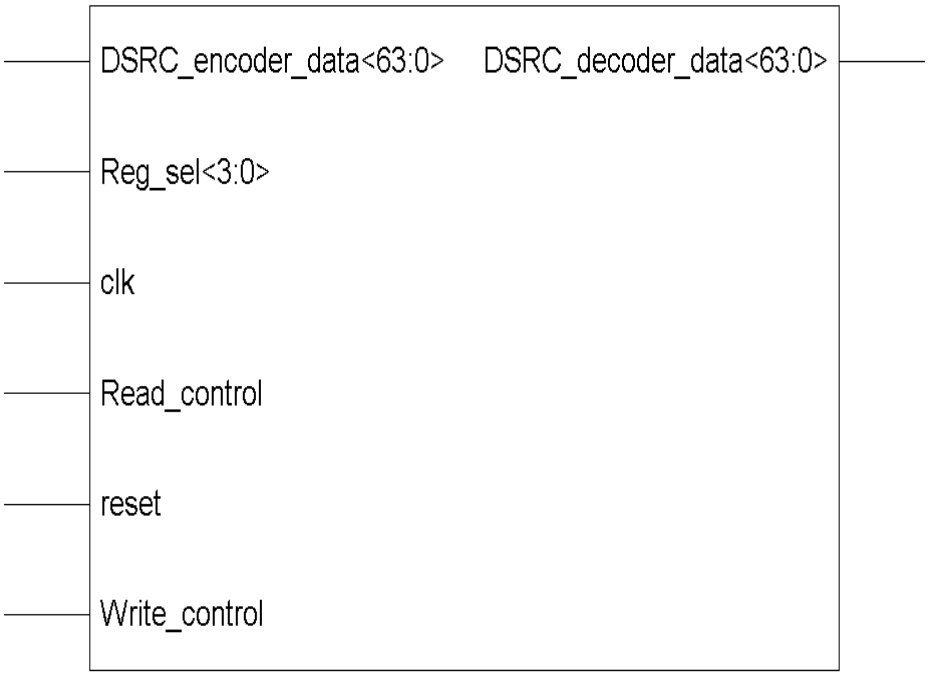


**Fig.7. Vehicular DSRC system**

The specific nature of vehicular ad hoc network makes this network different from other kind of networks. Some of its characteristics can be mentioned as follow: high mobility, short communication periods, limited bandwidth and the network has unpredictable characteristics such as its dynamic topology and signal strengths fluctuate with environment and time. Due to these unique features, providing an efficient data dissemination model is one of the most challenging areas in VANET

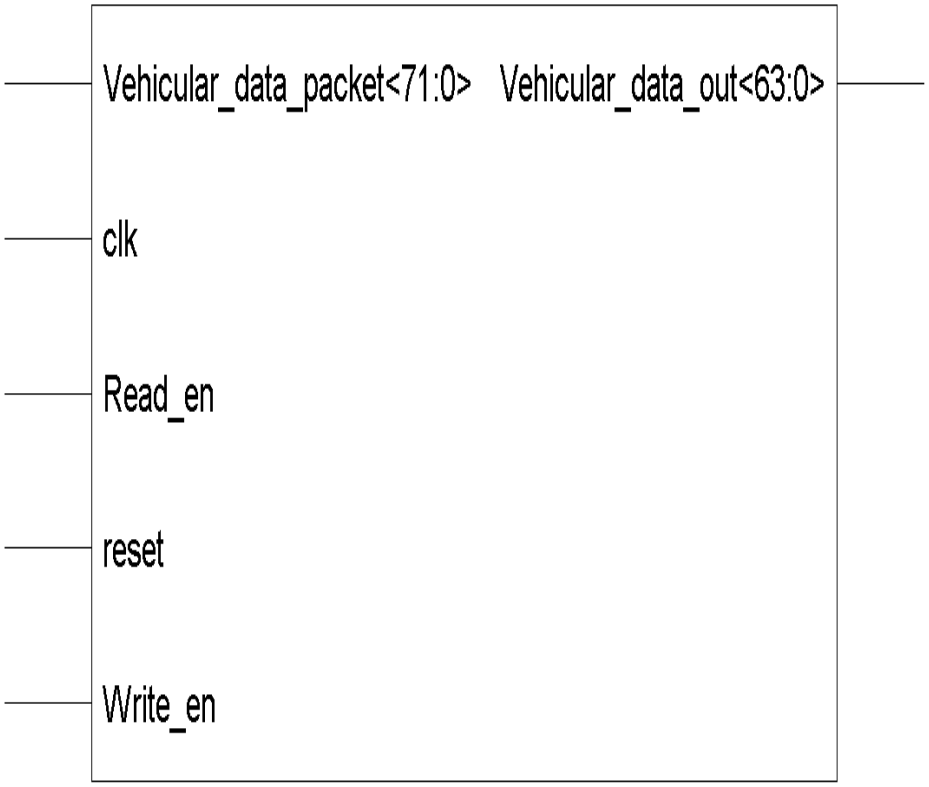
## (VI) RESULTS

RTL of DSRC SYSTEM –



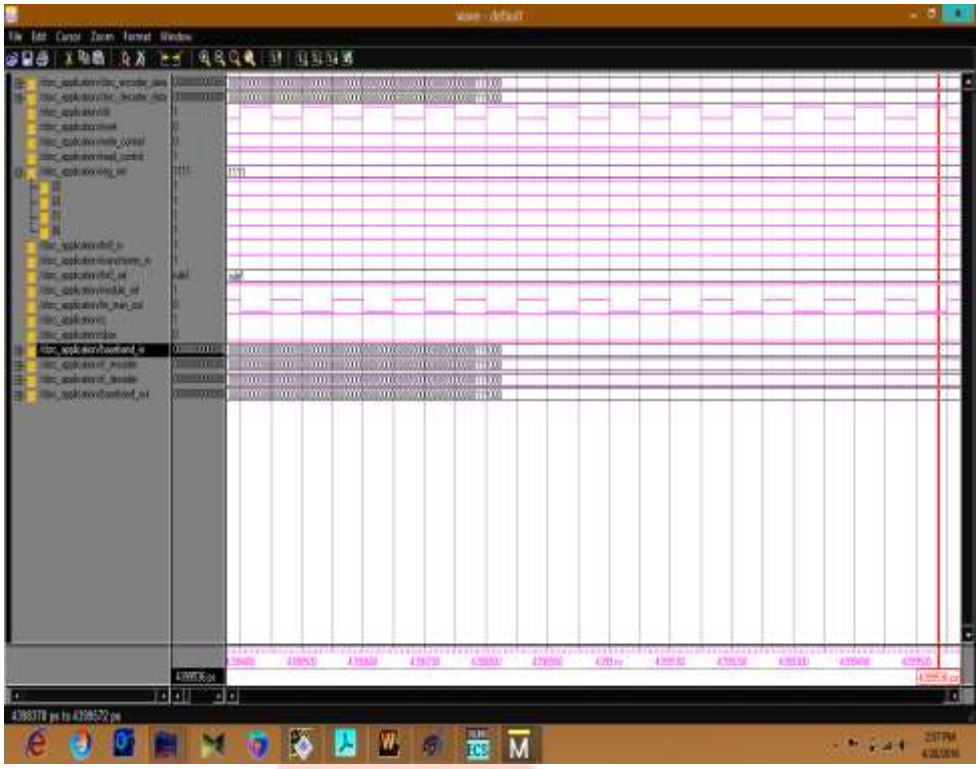

Here above figure is the RTL view of the DSRC SYSTEM

RTL of VEHICULAR DSRC

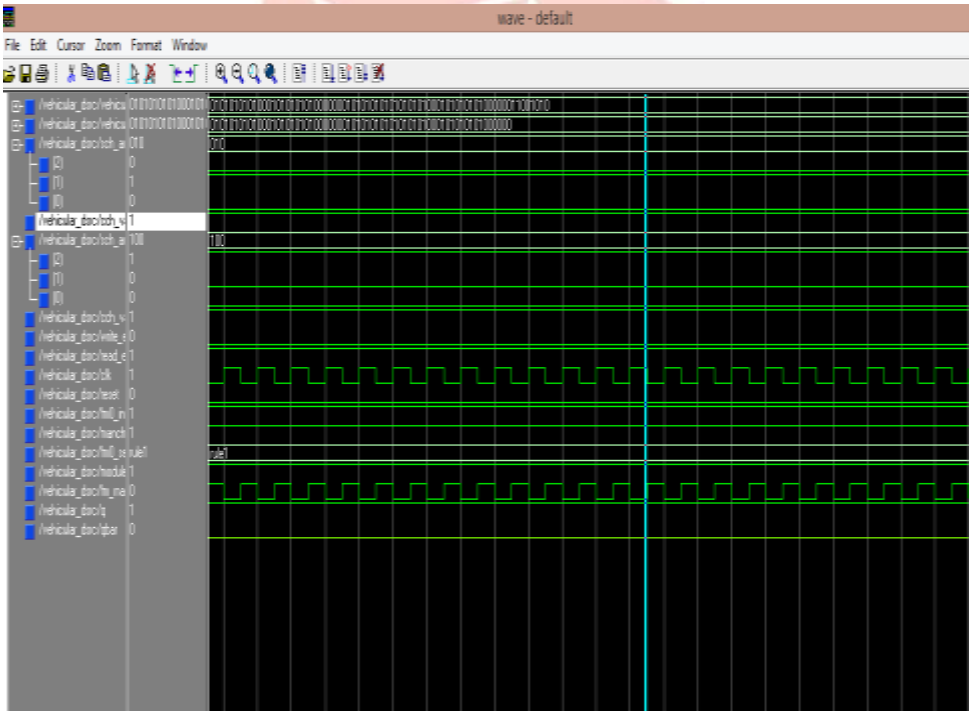



Here above figure is the RTL view of the VEHICULAR DSRC SYSTEM

**(VII) OUTPUT WAVEFORM**



This is the output waveform of DSRC SYSTEM according to the applied inputs.




This is the output waveform of VEHICULAR DSRC SYSTEM according to the applied inputs.

**(IX) CONCLUSION**

The proposed approach shows the concept of vehicular application used in short range communication. The vehicular DSRC i.e dedicated short range communication system using the vehicular model has been designed. Manchester encoder and FM0 encoder has been used as the encoding technique for the channel transmission. Dedicated short range communication system has been designed which consist of a transmitter and a receiver and a microprocessor . The microprocessor interprets instructions from media access control to schedule the tasks of baseband processing and RF front-end. The output is obtained using the modelsim software. The dedicated short range communication system is applied to the vehicular model and a vehicular dsrc system is designed by using VHDL hardware language with considering timing constraints. This paper presents the implementation with

regard to verilog language. Synthesizing and implementation (i.e. Translate, Map and Place and Route) of the code is carried out on Xilinx - Project Navigator, ISE 12.3i suite.

(X)**Acknowledgment**

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