Review Paper on Vedic Multiplier by Using Different Methods

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Abstract - In digital circuits multiplier has important role. These are the main important blocks in many applications like digital signal processing, microprocessor and microcomputers. The time that required to do calculation in multiplier is reduced by using Vedic multipliers. Vedic Mathematics is the fastest and low power multiplier. Vedic Mathematics have sixteen sutras but "Urdhva Tiryagbhyam" is mainly used .In this paper 16 bit Vedic multiplier is designed by using modified full adders which has used less number of slices and delay is reduced when compared to existing techniques of Vedic Multiplier. Simulation and synthesis are carried on XILINX ISE 14.4 software.

Keyword – Vedic Multiplier, Full Adder using Multiplexer, Ripple Carry Adder, VLSI.

I. INTRODUCTION

Vedic Mathematics is much simple and easy to understand. It also improves the speed of calculation. The word 'Vedic' is obtained from word "Veda" and its meaning is "store house of all knowledge". The Vedic multiplier has applications in microprocessors, filtering, Fourier transform, communication and Digital Signal Processing. Ancient Vedic mathematics consists of 16 Sutras that are related to different branches of mathematics like algebra, arithmetic and geometry. Vedic Multiplier mainly used "Urdhva Tiryagbhyam" (Vertically and Crosswise) which is used for both binary and decimal multiplication. This technique consists of generation of partial products and then performs addition simultaneously. This method can be used for 2x2, 4x4……NxN bit multiplication.

II. FULL ADDER USING HALF ADDERS

In this full adder it is design by using two half adders and an OR Gate. Inputs are 'a', 'b', 'cin' and outputs are 'sum' and 'carry'.

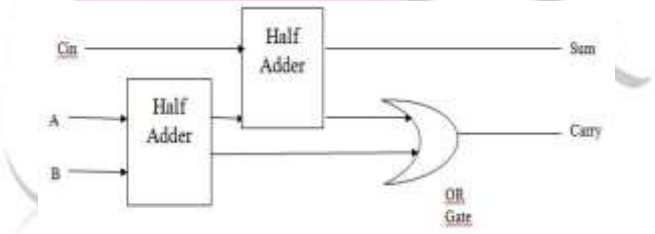

Fig.1: Full Adder using Half Adders

III. MODIFIED FULL ADDER 1

In this full adder it is design by using XOR Gate and 2:1 multiplexer. Inputs for XOR Gate are 'a', 'b', 'cin' and output is 'sum'. The inputs for multiplexer are 'b', 'cin' and select line is 's' and output is 'carry'.

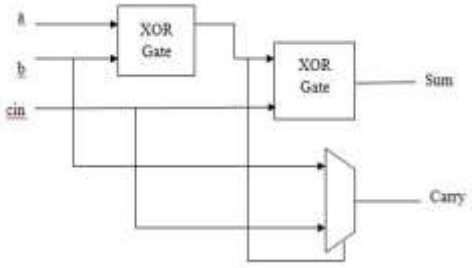

Fig.2: Modified Full Adder 1

IV. MODIFIED FULL ADDER 2

In this full adder two 4:1 multiplexer are used. Inputs for first multiplexer are 'c', 'not c', 'not c', 'c' and selection line are 'a' and 'b' and the output is sum. Whereas inputs for the second multiplexer are '0','c','c','1' and selection line are 'a' and 'b' and the output is 'carry'.

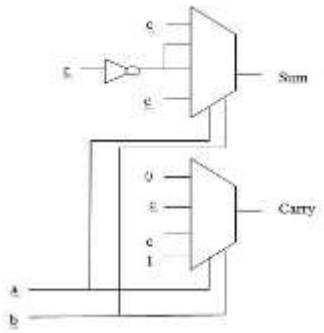

Fig.3: Modified Full Adder 2

V. MODIFIED FULL ADDER 3

In this full adder XOR Gate, XNOR Gate and 2:1 multiplexer is used. Inputs for XOR Gate are 'a' and 'b' and the intermediate output is y. Inputs for XNOR Gate are 'a' and 'b' and intermediate output is 'z'. Inputs for first multiplexer are 'y' and 'z' and selection line is 'cin'. Inputs for the second multiplexer are 'a', 'cin' and the selection line is 'y' and the output is 'carry'.

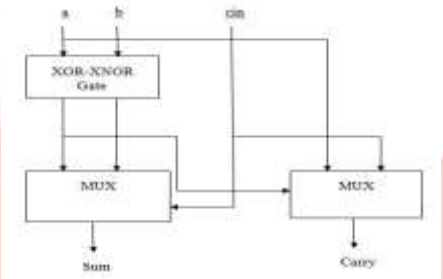

Fig.4: Modified Full Adder 3

VI. LITERATURE SURVEY

VijayaLakshmi Bandi et. al[1] develop "Performance Analysis For Vedic Multiplier Using Modified Full Adders". In this paper vedic multiplier is designed by using modified full adder which has used less number of slices and has less delay when compared to conventional vedic multiplier that is design by using BEC adder. The vedic multiplier using full adder1 has better performance when compared to other full adders. This design is simulated and synthesis in Xilinx ISE 12.2 software.

G. Challa Ram, D. Sudha Rani, Y. RamaLakshmanna, K.Bala Sindhuri et. al [2] develop "Area Efficient Modified Vedic Multiplier". In this paper vedic multiplier is designed by using Binary to Excess Converter. By using BEC adder the memory utilizing is less when compared to vedic multiplier. In this paper 8 bit and 16 bit vedic multiplier is proposed by using BEC adder. The delay of vedic multiplier is less than the array multiplier. The design is implemented using Xilinx 12.2 ISE tools on Spartan 3E Kit and programmed in Verilog HDL.

Paras Gulati, Harsh Yadav, Manoj Kumar Taleja et. al [3] develop "Implementation of an Efficient Multiplier Using the Vedic Multiplier Algorithm". In this paper 16 bit vedic multiplier is designed by using three different adders that are Modified Carry Select Adder, Ripple Carry Adder and Kogge Stone Adder. The results show that Modified Carry Select Adder is better in terms of speed and power consumption. The design is implemented in Xilinx software and synthesized by using Virtex-7 family, simulstion is performed in Modelsim and programmed in Verilog language.

M. Akila, C. Gowribala,S. Maflin Shaby et. al [4] develop "Implemention of High Speed Vedic Multiplier using Modified Adder". In this paper modified Carry Select Adder is used to improve the parameters like speed, delay and area.16 bit vedic multiplier is designed by using Xilinx software and results of this multiplier are compared with existing vedic multipliers.

Josmin Thomas, R. Pushpangadan, Jinesh S et. al [5] develop "Comparative Study of Performance Vedic Multiplier on The Basis of Adders Used". In this paper area, delay and power of vedic multiplier are compared. To choose the better adders from existing adders the parameters are compared by using Carry Look Ahead Adder(CLA), Carry Select Adder(CSLA), Ladner Fischer Adder(LFA), Brent Kung Adder(BKA), Kogge Stone Adder(KSA) and compressor. Carry Select Adder is better adder in terms of area and power consumption. Whereas Carry Look Ahead Adder is better in terms of speed.

Saji. M. Antony, S.Sri Ranjani Prashanthi, Dr. S. Indu, Dr. Rajeswari Pandey et. al [6] develop "Design of High Speed Vedic Multiplier Using Multiplexer Based Adder". In this paper vedic multiplier is designed by using multiplexer based adder. It has less delay and high speed when compared to other vedic multipliers. This design is simulated using ModelSim and synthesized using Xilinx ISE 14.7 software and programmed in Verilog.

Kokila Bharathi Jaiswal, Nithish Kumar, Pavithra Seshadri, Lakshminarayana G. et. al [7] develop "Low Power Wallace Tree Multiplier Using Modified Full Adder". In this paper modified full adder using multiplexer is designed to achieve low power consumption. The The designs are synthesized in Synopsys Design Compiler using SAED90nm CMOS technology. To analyze the efficiency of proposed design, the conventional Wallace tree multiplier structure is used. The design is programmed using Verilog HDL.

Bhavani Prasad.Y, Ganesh Chokkakula, Srikanth Reddy.P, Samhitha.N.R. et. al [8] develop "Design of Low Power and High Spped Modified Carry Select Adder for 16 bit Vedic Multiplier". In this paper 16 bit vedic multiplier is designed by using Modified Carry Select Adder. The results are compared with booth and array multiplier. It shows that the modified Carry Select Adder is better in terms of speed, area and delay. Simulation is done by using Modelsim, NCLaunch and programmed in Verilog HDL.

Manoranjan Pradhan, Rutuparna Panda, Sushant Kumar Sahu et. al [9] develop "Speed Comparsion of 16*16 Vedic multiplier". In this paper 16 bit Vedic multiplier using Nikhilam Sutra is designed. This multiplier has better speed when compared to Urdhva Tiryakbhyam. This design is simulated and synthesized using Xilinx ISE 10.1 software and programmed in VHDL. This multiplier is implemented on Spartan 2 FPGA device XC2S30-5pq208.

Sreehari Veeramachaneni, Kirthi M Krishna, Lingamneni Avinash, Sreekanth Reddy Puppala, M.B. Srinivas et. al[10] develop "Novel Architectures For High Speed and Low Power 3-2,4-2, and 5-2 Compressors". In this paper new compressor architecture has been proposed and compared with existing architectures. It gives better results in area, power and delay.

PROPOSED METHODOLOGY

In 16x16 bit multiplier, the multiplicand consists of 16 bits each. The result of multiplication is 32 bits. In this multiplier 8 bit Vedic multiplier, 16 bit adder and 24 bit adder is used. It consists of three sections. In which first set consists of a (7:0) and b(7:0), second set has a(15:8) and b(7:0), third set has a(7:0) and b(15:8) and fourth set consists of a(15:8) and b(15:8). The output of these is 16 bits. In second section one 16 bit adder and one 24 bit adder is used. In third section 24 bit adder is used. The output of second section is given to 24 bit adder. The output of this adder is (32:8). Lowest bits of output are taken from 8 bit Vedic multiplier output that is (7:0).The Final Output has 32 bits.

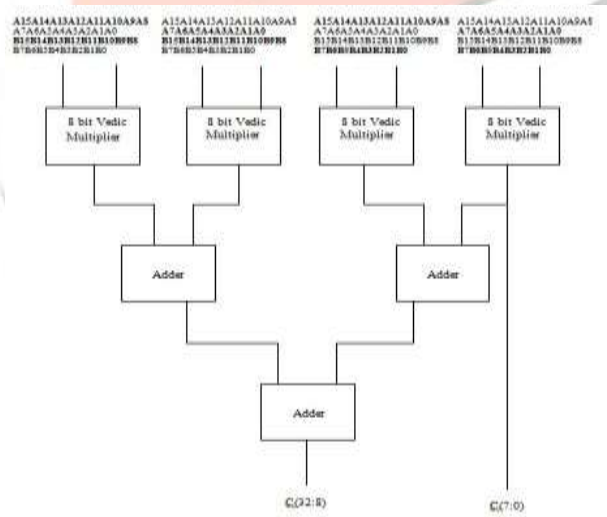

Fig.5:16 bit Vedic Multiplier

VII. CONCLUSION

This paper presents the survey of Vedic multiplier by using different adders. In this paper modified full adders are used to design 16 bit Vedic multiplier which will improve the performance of 8 bit Vedic multiplier by calculating delay and memory utilization.

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