16 Bit DLL Multiplier Using Low Power Pulse Generator

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***Abstract*— a highly faithful, high-speed and power efficient frequency multiplier is planned for a clock generator based on delay-locked loop to produce a multiplied clock with a max frequency range. The planned edge combiner attains a highly reliable and high-speed operation using flap canceller and hierarchical structure. In accumulation, by relating the logical work to the control logic design of multiplication-ratio and pulse generator, the planned frequency multiplier reduces the lag difference among negative and positive-edge propagation paths that cause a deterministic jitter. At last, a mathematical analysis is implemented to compare and examine the act of the planned frequency multiplier with that of previous frequency multipliers. The 0.18-µm CMOS process technology is customized to construct the desired frequency multiplier which is having the multiplication ratios of 1, 2, 4, 8, and 16 and an output range between 90 MHz to 3.2 GHz.**

***Index Terms*— Jitter, Delay-Locked Loop, flap canceller, multiplication ratio**

I. INTRODUCTION

Dynamic voltage and frequency scaling (DVFS) is as of now being utilized as a part of about each framework on-chip (SoC), in light of the fact that DVFS can effectively bring down the dynamic power utilization of the SoCs while keeping up the execution. DVFS, which recognizes the SoC workload and powerfully changes the supply voltage and frequency, requires a dc– dc converter and a clock generator. The clock generator is for the most part executed utilizing a stage bolted circle (PLL) to effortlessly change the yield clock frequency. Be that as it may, PLLs have a few shortcomings, for example, the trouble of outline, high-cost circle channels, and jitter aggregation. Delay-locked loops(DLLs) are a decent substitute for PLLs, in light of the fact that they resolve the PLL shortcomings; nonetheless, on the grounds that a DLL utilizes a defer line rather than an oscillator, its yield clock frequency is dependably the same as its info clock frequency. Subsequently, a DLL alone can't be utilized as a clock generator. A few DLL-based clock generators have been proposed to tackle this issue [4]– [9]. The DLL-based clock generator is made out of a DLL center and a frequency multiplier, and the frequency multiplier is for the most part isolated into two squares: 1) a heartbeat generator and 2) an edge combiner. On the off chance that variable frequency augmentation is required.

Increase proportion control rationale is included. The DLL center produces multiphase timekeepers utilizing a reference check in the DLL center. The beat generator produces the fitting number of heartbeats from the multiphase timekeepers as indicated by the duplication proportion control flag, and the edge combiner creates an increased clock utilizing the chose beats. When all is said in done, the most extreme augmentation proportion of the frequency multiplier is half of the quantity of multiphase timekeepers. Since the frequency multiplier produces the duplicated clock by just gathering the multiphase tickers, jitter amassing does not happen. Furthermore, the frequency multiplier can without much of a stretch change increase proportions. Be that as it may, to build the most extreme duplication proportion, the rationale profundity or yield stacking of the frequency multiplier must be expanded. Nonetheless, it extremely corrupts the most extreme increased clock frequency. To take care of the issues of the past frequency multiplier a novel frequency multiplier is proposed in this paper. A progressive structure and a cover canceller are utilized for the proposed edge combiner. Inferable from the proposed edge combiner, the proposed frequency multiplier can create a higher frequency and more extensive frequency go duplicated clock with lower control utilization for each frequency proportion and higher dependability than past frequency multipliers.

This frequency multiplier is made out of increase proportion control rationale, an AND-door based heartbeat generator, and a differential cascade voltage switch (SW) logic (DCVSL)- arrange based edge combiner. The frequency multiplier can produce the increased differential tickers with a little territory punishment. As just a single PD-N is added to every differential yield of the edge combiner when the greatest augmentation proportion is expanded by one, the bundle of the edge combiner increments gradual than that of the edge combiner.

II. RELATED WORK DONE

[2] In this paper they survey, the microprocessor system in portable electronic devices often has a time-varying computational load which is comprised of: (1) Figure out rigorous and stationary processes, (2) surroundings and high-latency processes, and (3) structure found idle. The fundamental design objectives for the processor systems in these applications are supplying the highest possible peak performance for the compute-intensive code while maximizing the battery life for the remaining low performance periods. If clock frequency and supply voltage are forcefully varied in response to computational load demands, then energy consumed per process can be shortened for low figuring periods, while remaining peak performance when required.

This operation, which bears the best possible energy efficiency for time-varying calculative loads, is called dynamic voltage scaling.

[3] This paper proposes high complication and time-varying workload of developing multimedia applications possess a major challenge for (DVS) algorithms. For real time application many DVS algorithms have been proposed which is productive method to classify such DVS algorithms by excellent multimedia application which does not exist. In this paper, they propose the new offline linear programming method to regulate the low energy utilization for processing multimedia tasks under delay deadlines. On the basis of the accessed energy lower bound, they analyzed excellence of DVS algorithms. Afterword, they boost the LP formulation in order to construct an online DVS algorithm for real-time multimedia processing based on powerful sequential linear programming. Simulation results collected by decoding broad range of video sequences shows that, on average, our online algorithm gives organized solution that have need of 0.3% more energy. In comparison, a very latter algorithm obsesses approximately 4% more energy than the flawless lower bent at the same missing rate.

[4] Here we study traditional voltage escalating system, require a delay margin to continue a certain level of firmness across all possible device and wire process deviations and temperature inconstancy. This margin is required to canvas for a possible change in the critical path due to such changes. Moreover, a critical path changes from one operating voltage to one another due to slower interconnect delay arises with voltage compared to logic delay. To assure a fault free operation with high limit both process variation and interconnect delay are in challenging with technology scaling. Such margin is rendered into voltage upward and corresponding energy inadequately. Moreover, voltage scaling characteristics of the certain critical path is firmly followed by programming logic and interconnects delay lines to carry out same delay sequences as the actual critical path. Correlated to regular open-loop and closed-loop systems, the planned system is up to 39% and 24% more energy competent, respectively. A 0.18 µm technology test chip is deliberate to validate the functionality of the planned system showing critical path tracking.

[5] In this paper, a delay-locked loop (DLL)-based clock generator is presented has several inherent advantages over conventional phase-locked-loop-based generator, i.e, no jitter growth, quick locking, balanced loop production and easy combination of the loop filter.DLL based clock generator requires a fresh reference signal. To conquer limited locking range and frequency multiplication problem of the conservative DLL-based system here they suggest a phase detector with reset circuitry and a novel frequency multiplier. It is made-up in a 0.35µm CMOS process. Our DLL-based clock initiator covers 0.07 µm of area and consumes 42.9 mW of power. It has operation range of 120 MHz-1.1 GHz and it poses an exact cycle-to-cycle jitter at 1 GHz. The die area, peak-to-peak, and R.M.S. jitter are the three smallest comparison parameter. These parameter are related to those of high-frequency clock multipliers.

[6] This paper proposes a frequency multiplier composed by DLL method posse's monolithic CMOS local oscillator which organizes a 900-MHz carrier frequency with a low noise. The example, achieved in a multi-poly five-metal 0.35-/spl mu/m CMOS technology, achieves a -123 and -127 dBc/Hz phase noise at 60 and 330 kHz offset frequencies, respectively, while dissipating 130 mW from a 3.3-V supply. This example gives more support to fascinate the necessity of the IS-137 AMPS/TDMA dual-mode standard.

[7] A delay-locked loop (DLL)-based frequency synthesizer is designed for the ultra-wideband (UWB) Mode-1 system. This frequency synthesizer achieves less than 9.5-ns settling time with appropriate 528-MHz input reference frequency. This reference frequency utilizes wide loop bandwidth and rapid selling architecture. Furthermore, a discrete-time model and an analytical model of the DLL are anticipated here for phase noise in this work. Investigational results show great reliability with predicted settling time and phase noise. The circuit has been made-up in a 0.18-/spl mu/m CMOS technology and consumes only 54 mW from a 1.8-V supply. It display a sideband magnitude of -35.4 dBc and -120-dBc/Hz phase noise at the frequency offset of 1 MHz.

III. OBJECTIVES

To achieve the planned edge combiner with a highly reliable and high-speed operation using an overlap canceller and categorized structure.

In addition, by relating the logical exertion to the multiplication-ratio of control logic design and pulse generator, the planned frequency multiplier reduces the delay difference among negative-edge and positive-edge propagation paths, which causes a deterministic jitter.

IV. PROBLEM STATEMENT

Earlier the frequency multiplier has more delay, where PLL is used to change output frequency. Also structure is not faithful for high speed and efficient power consumption. Previously pulse generator could not be controlled logically. Jitter accumulation problem for overlapping clocks was also there, because of frequency multiplier which creates multiplied clock by simply collecting the multiphase clock.

V. PROPOSED SYSTEM

The planned clock generator based on DLL is series of the programmed frequency multiplier and a DLL core, as shown in Fig.5.1. To improve the lock time, which is an imperative design constraint in the clock generator, a dual-edge-triggered phase-detector-based DLL core is adopted. Alike to previous frequency multipliers, the projected frequency multiplier are also serene of an edge combiner, multiplication-ratio control logic and pulse generator.

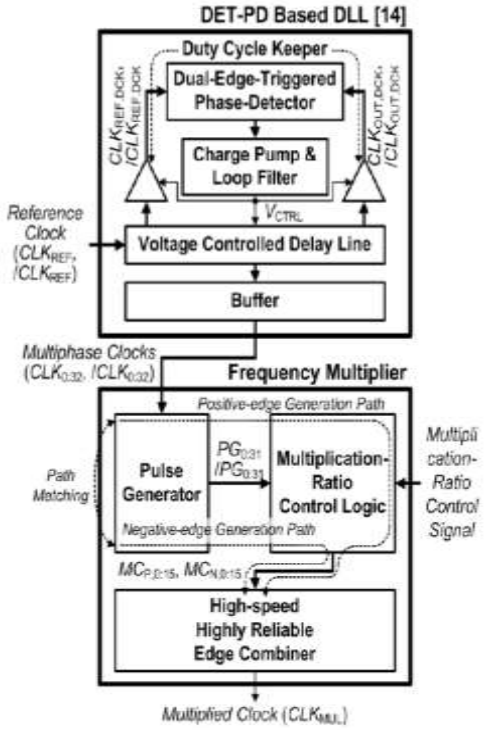

Fig.5.1 Structure of the proposed clock generator

Fig. 5.2 shows the operations of the planned frequency multiplier and the DLL. The dual-edge-triggered phase-detector equates both the negative and the positive edges of CLKOUT, DCK, and CLKREF, DCK which are recovered clocks duty cycle of output clock and reference clock using duty-cycle ranger. Within 300 cycles the DLL is locked in all process–voltage–temperature corners creates 32-phase differential clocks due to the dual-edge finding characteristic. The pulse creator marks pulses by using 32-phase differential clocks, for negative and positive-edge generation. Finally, the highly faithful and high-speed edge combiner generates one multiplied clock with the aid of all the outputs of the multiplication ratio control logic. Here the final multiplication ratio is 16 as the number of multiphase predefined was 32.

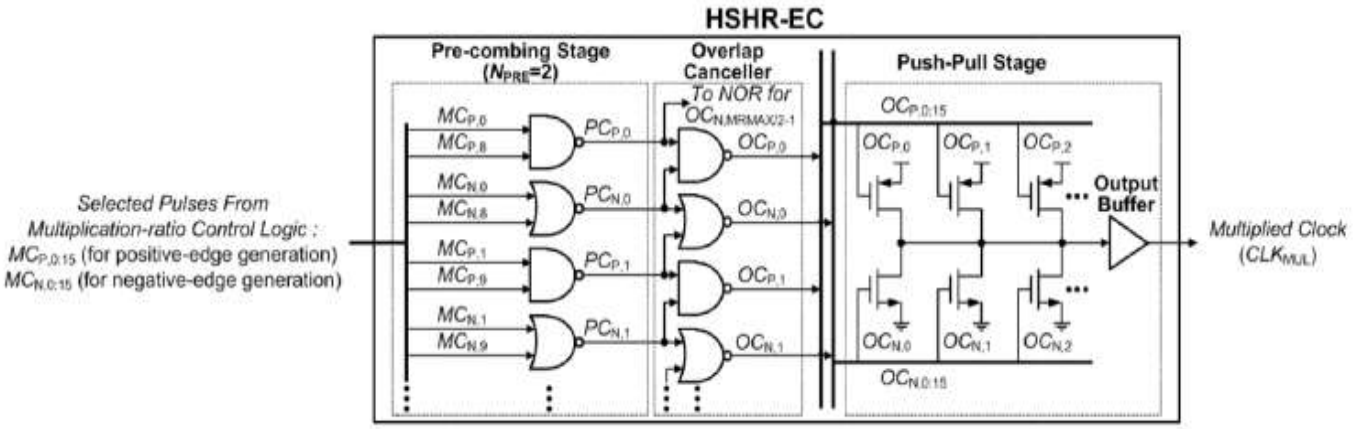

Fig.5.2. Structure of the proposed HSHR-EC.

To cure the reliability and the speed issues of earlier HSHR-EC edge combiners, which consists of an overlap canceller, push–pull stage and pre-combining stage, as shown in Fig.5.2, is projected. The push–pull stage, dual-step edge combiner, and pre-combining are used to improve the multiplied clock frequency to maximum. The overlay canceller is used to guarantee the steady operation of the frequency multiplier.

As is true for the frequency multipliers, the planned frequency multiplier might undergo from pulse overlapping due to the multiplication-ratio control logic. To stop this, an overlap canceller is implanted among the pre-combing and the push–pull stages. Its function is also shown in Fig. 5.3. As shown in Fig 5.2 the overlap canceller made up of simple NAND and NOR gates.

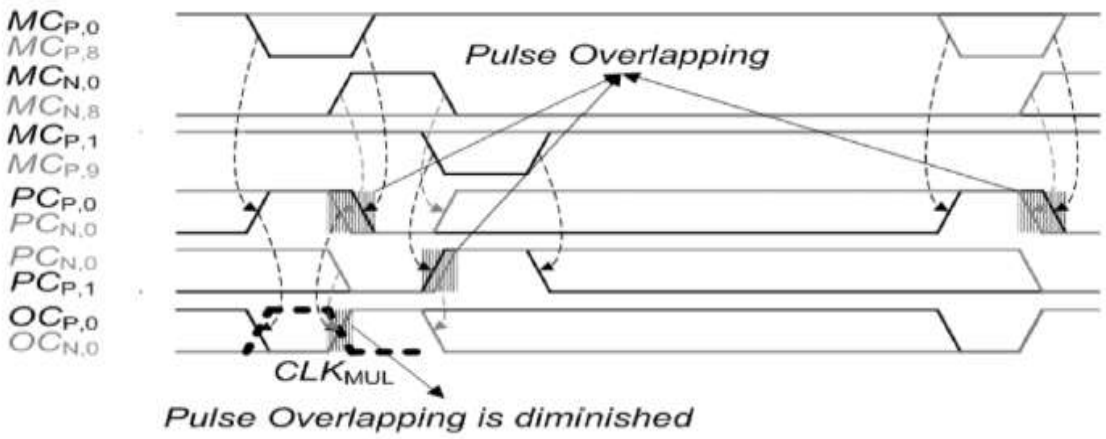

Fig. 5.3 Function of a proposed HSHR-EC

VI. CONCLUSION

This project designs a frequency multiplier for a clock generation. High speed operation gets achieved through suggested HSHC-EC which assured through edge combiner circuit. It provides reliable operation due to use of overlap canceller. To cut down delay difference among positive and negative edge propagation paths, the increased pulse generator and multiplication control logic are proposed. At last to get multiplication ratio such as 1,2,4,8 and 16 with output domain of 90 MHz-3.2 GHz, the frequency multiplier is fabricated using 0.18 µm CMOS process technology.

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