Design Of Less Voltage Quadrupler DC Converter With A Low Stress Voltage Switch Transformer

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***Abstract* - In this paper, a novel transformer-less adjustable voltage quadrupler dc–dc converter with high-voltage transfer gain and reduced semiconductor voltage stress is proposed. The pro-posed topology utilizes input-parallel output-series configuration for providing a much higher voltage gain without adopting an ex-treme large duty cycle. The proposed converter cannot only achieve high step-up voltage gain with reduced component count but also reduce the voltage stress of both active switches and diodes. This will allow one to choose lower voltage rating MOSFETs and diodes to reduce both switching and conduction losses. In addition, due to the charge balance of the blocking capacitor, the converter fea-tures automatic uniform current sharing characteristic of the two interleaved phases for voltage boosting mode without adding extra circuitry or complex control methods. The operation principle and steady analysis as well as a comparison with other recent exist-ing high step-up topologies are presented. Finally, some simulation and experimental results are also presented to demonstrate the effectiveness of the proposed converter.**

***keywords* - Automatic uniform current sharing, high step-up converter, low voltage stress, transformer-less, voltage quadrupler**

I. INTRODUCTION

With global energy shortage and strong an Environmental movements, renewable or clean energy sources such as solar cells and fuel cells are increasingly valued worldwide. However, due to the inherent low voltage characteristic of these sources, a high step-up dc converter is essential as a prestage of the corresponding power conditioner. The conventional boost and buck–boost converters, due to the degradation in the overall efficiency as the duty ratio approaches unity [1], obviously can-not fulfill the application need. Besides, the extreme duty ratio not only induces very large voltage spikes and increases con-duction losses but also induces severe diode reverse-recovery problem [2], [3]. Many topologies have been presented to pro-vide a high step-up voltage gain without an extremely high duty ratio as can be seen from the review paper [4]. A dc–dc fly-back converter is a very simple isolated structure with a high step-up voltage gain, but the active switch of this converter will suffer a high voltage stress due to the leakage inductance of the transformer. For recycling the energy of the leakage inductance and minimizing the voltage stress of the active switch, some energy-regeneration techniques have been proposed to clamp the voltage stress on the active switch and to recycle the leakage-inductance energy [5]–[7]. Some existing isolated voltage-type converters, such as the phase-shifted full-bridge converters, can achieve a high step-up gain by increasing the turns ratio of the transformer. Unfortunately, the higher input current ripple will reduce the maximum output power and shorten the usage life of input electrolytic capacitor. To reduce the effects, more input electrolytic capacitors are required to suppress the large input current ripple. Furthermore, the output diode voltage stress is much higher than the output voltage, which will degrade the circuit efficiency in the high-output-voltage applications. Other isolated current-type converters, such as the active-clamp dual-boost converters and the active-clamp full-bridge boost con-verters [8], [9], can realize high efficiency and high step-up conversion. However, the start-up operation of these converters must be considered separately. Moreover, the cost is increased because many extra power components and isolated sensors or feedback controllers are required. In order to reduce system cost and to improve system efficiency, a nonisolated dc/dc converter is, in fact, a more suitable solution [10], [11].

The switched capacitor-based converters proposed in [12]–[15] provide solutions to improve the conversion effi-ciency and achieve large voltage conversion ratio. Unfortu-nately, the conventional switched capacitor technique makes the switch suffer high transient current and large conduction losses. Furthermore, many switched capacitor cells are required to ob-tain extremely high step-up conversion, which increases the circuit complexity [27]. However, recently a study on energy ef-ficiency of switched-capacitor converters was presented in [33]; the authors presented some design rules useful for developing high-efficiency switched-capacitor converters, based on their analysis. In [34], several modular converter topologies were presented based on a switched-capacitor cell concept in which a soft-switched scheme was used to reduce the switching loss and electromagnetic interference [35], [36].

The coupled inductor-based converters are another solution to implement high step-up gain because the turns ratio of the coupled inductor can be employed as another control freedom to extend the voltage gain [16]–[18], [29], [31]. However, the input current ripple is relatively larger by employing single-stage single-phase-coupled inductor-based converters, which may shorten the usage life of the input electrolytic capaci-tor [27]. As such, a family of interleaved high step-up boost converters with winding-cross-coupled inductors is proposed in [19]–[21], [30]. The active clamp or passive lossless clamp circuits are adopted to achieve soft-switching operation. Alter-natively, some interleaved high step-up converters with simpli-fied coupled inductors are introduced to derive more compact circuit structure [22], [23], [32].

The interleaved voltage doubler [24] has been proposed for universal line power factor correction front end with automatic

current sharing capability and lower active switch stress to in-crease the low-line efficiency. However, the voltage gain is not high enough and the diode voltage stress remains very high [28]. To achieve higher voltage conversion ratio and further reduce voltage stress on the switch and diode, the high step-up ratio con-verter [25] and the ultrahigh step-up converter [26] have been proposed. These converters can provide large step-up voltage conversion ratios. Unfortunately, the voltage stress of diodes in those converters remains rather high.

In this paper, a novel transformer-less adjustable voltage quadrupler topology is proposed. It integrates two-phase in-terleaved boost converter to realize a high voltage gain and maintain the advantage of an automatic current sharing capa-bility simultaneously. Furthermore, the voltage stress of active switches and diodes in the proposed converter can be greatly reduced to enhance overall conversion efficiency.

The remaining contents of this paper may be outlined as follows. First, the novel circuit topology and operation princi-ple are given in Section II. Then, the corresponding steady-state analysis is made in Section III to provide some basic converter characteristics. A prototype is then constructed and some simulation and experimental results are then presented in Section IV for demonstrating the merits and validity of the pro-posed converter. Finally, some conclusions are offered in the last section

II. OPERATING PRINCIPLE OF THE PROPOSED CONVERTER

For convenient reference, the two-phase interleaved boost converter with parallel-input series-output connection is first shown in Fig. 1(a). The proposed converter topology is basi-cally derived from a two-phase interleaved boost converter and is shown in Fig. 1(b). Comparing Fig. 1(a) with Fig. 1(b), one can see that two more capacitors and two more diodes are added so that during the energy transfer period partial inductor stored energy is stored in one capacitor and partial inductor stored en-ergy together with the other capacitor store energy is transferred to the output to achieve much higher voltage gain. However, the proposed voltage gain is twice that of the interleaved two-phase boost converter. Also, the voltage stress of both active switches and diodes are much lower than the latter. Furthermore, as will be obvious latter, the proposed converter possesses automatic uni-form current sharing capability without adding extra circuitry or complex control methods. The detailed operating principle can be illustrated as follows. The proposed converter topology, like any existing high step-up dc converter, possesses the drawback of existence of pulsating output period. Furthermore, as the main objective is to obtain high voltage gain and such characteristic can only be achieved when the duty cycle is greater than 0.5 and in continuous con-duction mode (CCM);

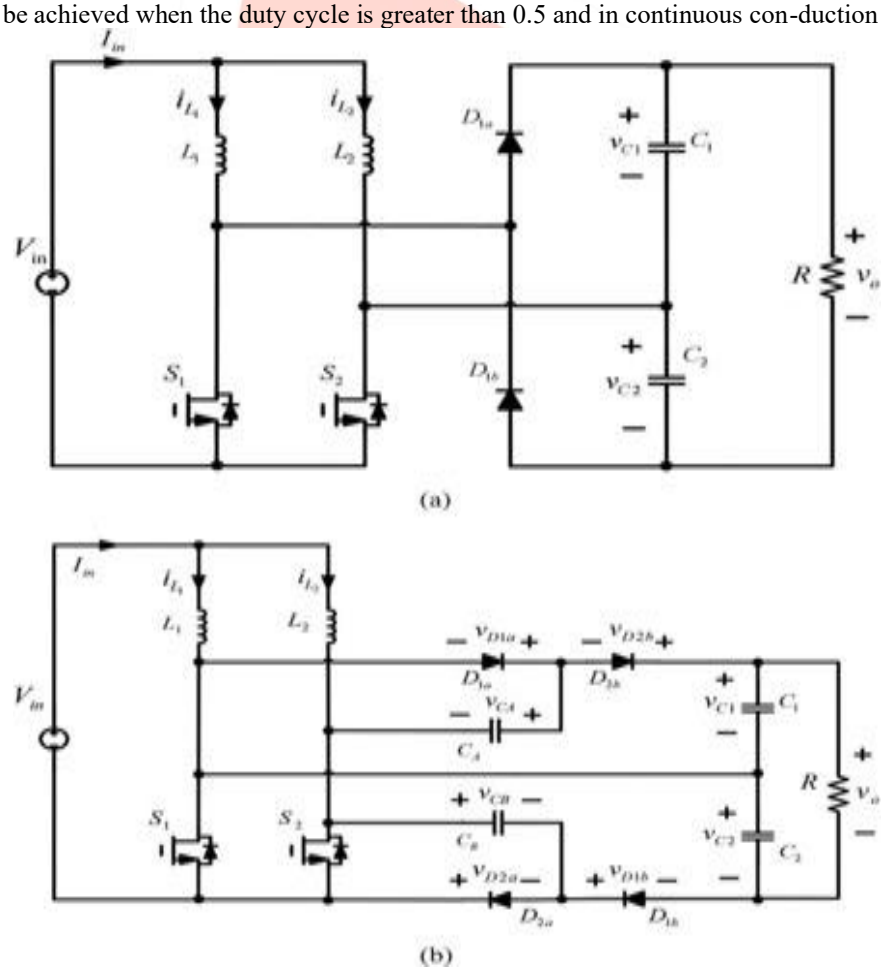


Fig. 1. Configurations of (a) two-phase interleaved boost converter (b) the proposed converter

hence, the steady-state analysis is made only for this case. However, with duty cycle lower than 0.5 or in DCM, as there is no enough energy transfer from the inductors to the blocking capacitors, output capacitors, and load side, and consequently it is not possible to get the high voltage gain as that for duty ratio greater than 0.5. In addition, only with duty cycle larger than 0.5, due to the charge balance of the blocking ca-pacitor, the converter can feature the automatic current sharing characteristic that can obviate any extra current-sharing control circuit. On the other hand, when duty cycle is smaller than 0.5, the converter does not possess the automatic current sharing ca-pability any more, and the current-sharing control between each phases should be taken

into account in this condition. In order to simplify the circuit analysis of the proposed con-verter, some assumptions are made as follows

Basically, the operating principle of the proposed converter can be classified into four operation modes. The interleaved gating signals with a 180 ◦ phase shift as well as some key operating waveforms are shown in Fig. 2.

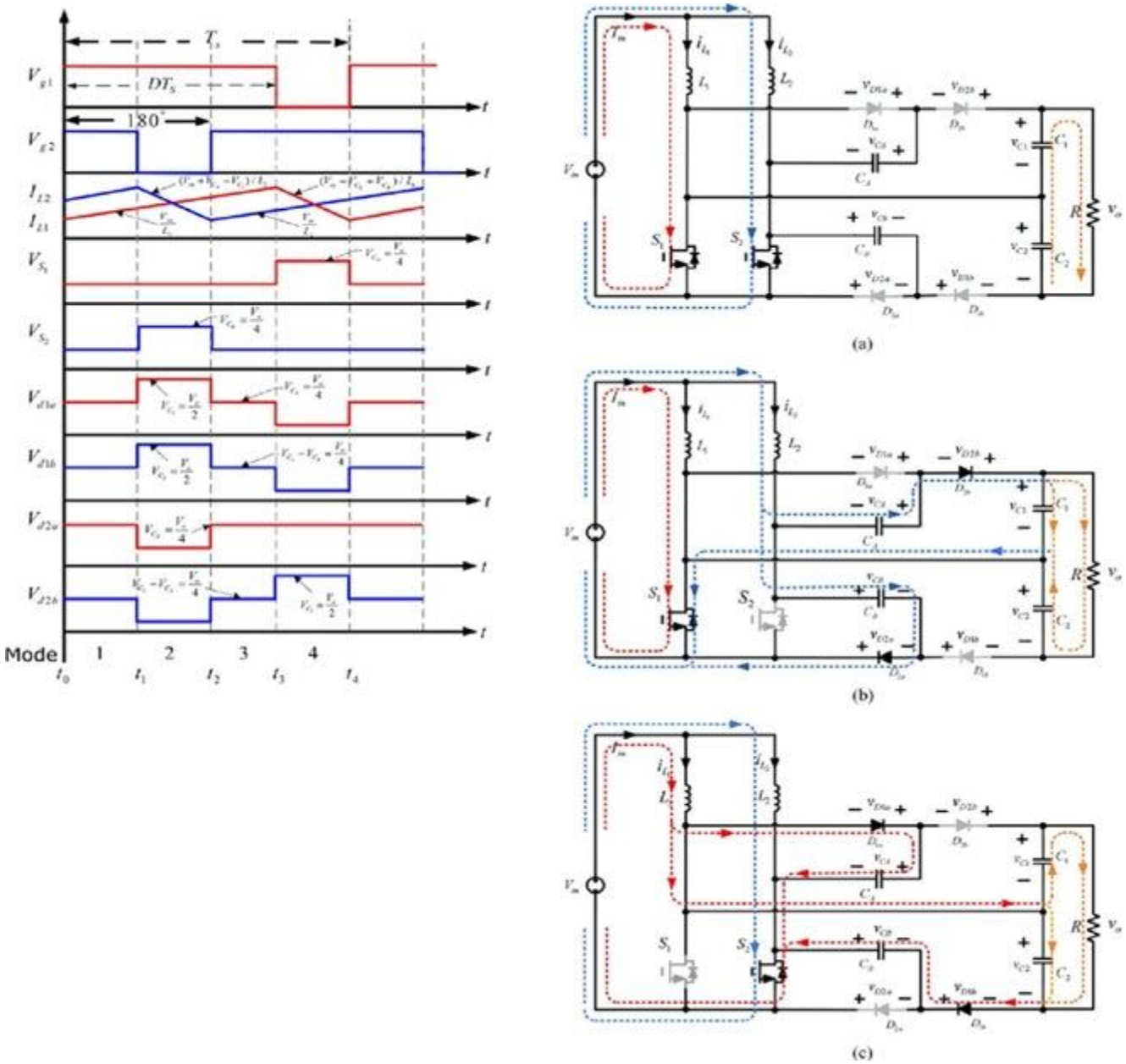


Fig. 3. Equivalent circuit of the proposed converter (a) Mode 1 and 3 (b) Mode 2 (c) Mode 4.

Mode 1 ($t_0 \le t < t_1$): For mode 1, switches S_1 and S_2 are turned ON, D_{1a} , D_{1b} , D_{2a} , D_{2b} are all OFF. The corresponding equivalent circuit is shown in Fig. 3(a). From Fig. 3(a), it is seen that both i_{L1} and i_{L2} are increasing to store energy in L_1 and L_2 , respectively. The voltages across diodes D_{1a} and D_{2a} are clamped to capacitor voltage $V_{C\,A}$ and $V_{C\,B}$, respectively, and the voltages across the diodes D_{1b} and D_{2b} are clamped to $V_{C\,2}$ minus $V_{C\,B}$ and $V_{C\,1}$ minus $V_{C\,A}$, respectively. Also, the load power is supplied from capacitors C_1 and C_2 . The corresponding state equations are given as follows

L1 {dL1/dt}=Vin

L_2 {dL2/dt}=V_{in}

Ca(dVca/dt}=0

Cb(dVcb/dt}=0

C1(dVc1/dt}=-(Vc1+ Vc2)/R

C2(dVc2/dt}=-(Vc1+ Vc2)/R

Mode 2 ($t_1 \le t < t_2$): For this operation mode, switch S_1 remain conduting and S2 Turened ofdiode D2a and D2b become conducting the correponding equvalient circuit is hown in fig

MODE 3: for thi operation a can be observed from fig 3.both s1 and s2 are turened ON.the corresponding equivalent circuit turn out be the same as fig 3a).

MODE 4:

For this operation mode, switch s2 remains conducting s1 I turned off,diode D1a and D1b become conducting.the coreponding equivalent circuit is shown in figer

L1 {dL1/dt}=Vin-V_{ca}
L_2 {dL2/dt}=V_{in}
Ca(dVca/dt}=I_{ca}+I_{l1}
Cb(dVcb/dt}= I_{ca}-I_{l1}
C1(dVc1/dt}=-(Vc1+ Vc2)/R
C2(dVc2/dt}=-(Vc1+ Vc2)/R

III. STEADY-STATE ANALYSIS

In order to simplify the circuit performance analysis of the proposed converter in CCM, the same assumptions made in the previous section will be adopted

A. Voltage Gain:

Referring to Fig. 3(a) and (c), from the volt–second rela tionship of inductor L_1 (or L_2), one can obtain the following relations:

$$V_{in} D + (V_{in} - V_{CA})(1 - D) = 0$$
$$V_{in} D + (V_{in} - V_{CB})(1 - D) = 0$$

Also from the equivalent circuits in Fig. 3(b) and (c), voltage V_{C1} and V_{C2} can be derived as follows by substituting the V_{Ca} and Vcb

$$V_{C1} = V_{CA} + V_{CB} = 2/(1\text{-}D)Vin$$
$$V_{C2} = V_{CA} + V_{CB} = 2/(1\text{-}D)Vin$$

Output voltage ntain by

$$V_o = V_{C1} + V_{C2} = 4/(1\text{-}D)Vin$$

B. Voltage Stresses on Semiconductor Components

To simplify the voltage stress analyses of the components of the proposed converter, the voltage ripples on the capacitors are ignored. From Fig. 3(b) and (c), one can see that the voltage stresses on active power switches S_1 and S_2 can be obtained

$^{V}S_{1,max} = {}^{V}S_{2,max} = 1/(1\text{-}D)Vin$

the voltage stresses on the active power switches can be expressed as

$^{V}S_{1,max} - VS_{2,max} = Vo/4$

In fact, one can see from (27) that the maximum resulting voltage stress of diodes is equal to Vo /2. Hence, the proposed converter enables one to adopt lower voltage rating diodes to further reduce conduction losses

C. Characteristic of Uniform Input Inductor Current Sharing

By using the state space averaging technique, one can repeat the previous process to get the averaged state equations quite straightforward as follows:

$$L_1 \frac{di_{L1}}{dt} = V_{in} - (1 - D)V_{CA} \quad (28)$$

$$L_2 \frac{di_{L2}}{dt} = V_{in} - (1 - D)V_{CB} \quad (29)$$

$$C_A \frac{dv_{CA}}{dt} = \frac{(1 - D)C_A (C_{eq1} I_{L1} (C_2 + C_B) - C_{eq2} I_{L2} C_1)}{c_{eq1}\, c_{eq2}} - \frac{(1 - D)C_A C_B (C_{eq1} + C_{eq2})(V_{C1} + V_{C2})}{{}^{C}_{eq1}\, {}^{C}_{eq2}\, R} \quad (30)$$

$$C_B \frac{dv_{CB}}{dt} = \frac{(1 - D)C_B (C_{eq2} I_{L2} (C_1 + C_A) - C_{eq1} I_{L1} C_2)}{c_{eq1}\, c_{eq2}} - \frac{(1 - D)C_A C_B (C_{eq1} + C_{eq2})(V_{C1} + V_{C2})}{{}^{C}_{eq1}\, {}^{C}_{eq2}\, R} \quad (31)$$

$$C_1 \frac{dv_{C1}}{dt} = \frac{(1 - D)C_1 (C_A I_{L2} R - (C_A + C_B)(V_{C1} + V_{C2}))}{c_{eq1}\, R} - \frac{D(V_{C1} + V_{C2})}{R} \quad (32)$$

$$C_2 \frac{dv_{C2}}{dt} = \frac{(1 - D)C_2 (C_B I_{L1} R - (C_A + C_B)(V_{C1} + V_{C2}))}{R C_{eq2}}$$

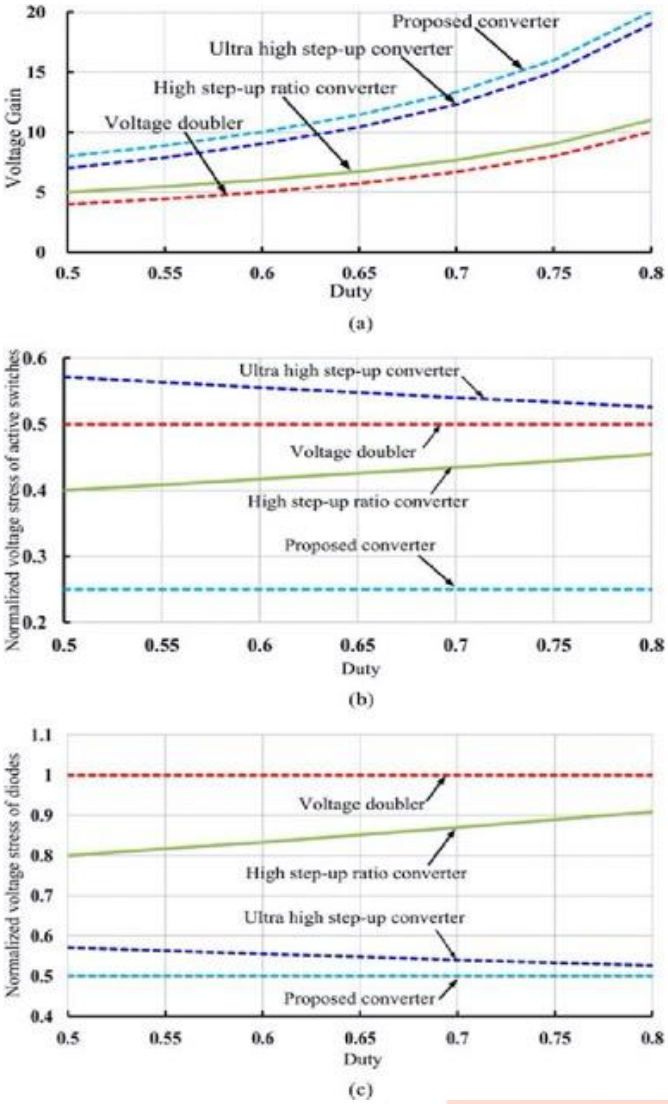
$$- \frac{D\,(V_{C1} + V_{C2})}{R} \qquad (33)$$

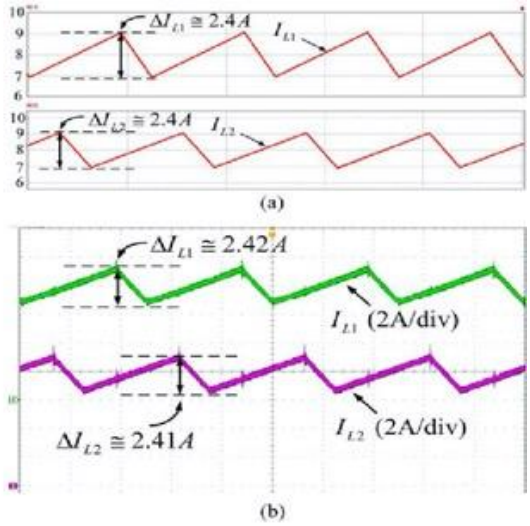
D. Performance Comparison

For demonstrating the performance of the proposed converter, the proposed converter is compared with some recent high step-up converters introduced in [24]–[26] as shown in Table I. shows the corresponding characteristic curve of the proposed converter. For comparison, the voltage stress is normalized by the output voltage Vo , the voltage gains, the normalized switch stresses and the normalized output diode stresses of the conventional voltage-doubler [24], high step-up ratio converter [25], and the ultrahigh step-up converter

It is seen from Fig. 4(a) that the proposed converter can achieve higher voltage gain than that of the other three boost converters. Therefore, the proposed converter is rather suitable for use in applications requiring high step-up voltage gain. From Fig. 4(b), one can see that the proposed converter can achieve the lowest voltage stress for the active switches.. As a result, one can ex-pect that with proper design, the proposed converter can adopt switch components with lower voltage ratings to achieve higher efficiency.

Gain/stress	Voltage Doubler [24]	High step-up ratio converter [25]	Ultra high step-up converter [26]	Proposed converter
Voltage gain	$\frac{2}{(1-D)}$	$\frac{3-D}{(1-D)}$	$\frac{3+D}{(1-D)}$	$\frac{4}{(1-D)}$
Voltage stress of switches	$\frac{1}{2}$	$\frac{1}{(3-D)}$	$\frac{2}{(3+D)}$	$\frac{1}{4}$
Voltage stress of diodes	1	$\frac{2}{(3-D)}$	$\frac{2}{(3+D)}$	$\frac{1}{2}$
numbers of MOSFETs	2	2	1	2
numbers of inductors	2	2	2	2
numbers of diodes	2	3	5	4
numbers of capacitors	2	3	4	4





IV. SIMULATION AND EXPERIMENTAL RESULTS

The To facilitate understanding the merits and serve as a verification of the feasibility of the proposed converter, a prototype with 25-V input, 400-V output**,** and 400-W rating is constructed.the interleaved tructure can effective increae the switching frequency and reduce the ouptut and input ripple as well as the storega of energy.

Similarly, to check the correctness of (26), experiments are made and the results are shown in Fig. 8. From Fig. 8, one can observe that the voltage stress of active switches is equal to one fourth of the output voltage. Also, to check the voltage stress of blocking capacitors, one can see when the proposed converter is operated in modes 2 and 4, the voltages of capacitors C_A and C_B are clamped at $_{1V-\text{in}D}$, and when the proposed converter is operated in modes 1 and 3, all diodes are OFF, and capacitors C_A and C_B are isolated as open circuits; The diode voltage waveforms of the simulation and exper-imental results are shown in Fig. 9, which indicates that the maximum voltage cross diodes $V_{D\ 1a}$, $V_{D\ 1b}$, and $V_{D\ 2b}$ equals 200 V which is indeed equal to one-half of the output voltage. The maximum voltage crosses diode $V_{D\ 2a}$ is 100 V which is equal to one fourth of the output voltage as expected.The diode current waveforms of the simulation and experi-mental results are shown in Fig. 10. In the proposed topology, low-voltage-rating rectifier diodes are used to reduce the con-duction loss. Due to the help of the blocking capacitor, the output current ripples are reduced.

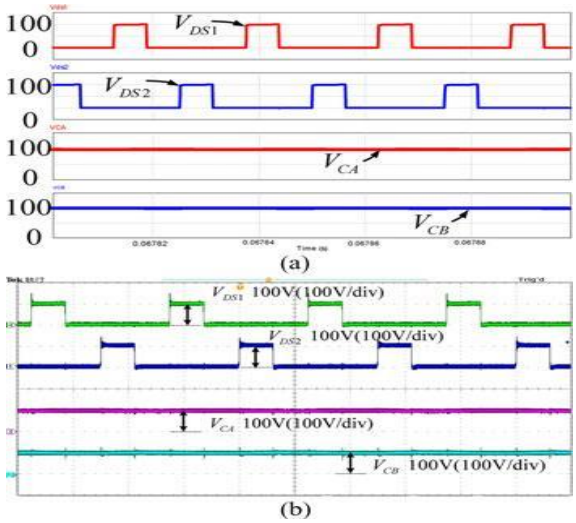


Fig. Waveforms of the voltage stress of V_{DS1}, V_{DS2}, V_{CA}, and V_{CB}

V. CONCLUSION

In this paper, a novel transformer-less adjustable voltage quadrupler dc–dc converter with high voltage transfer gain and reduced semiconductor voltage stress is proposed. The proposed topology utilizes input-parallel output-series configuration and is derived from a two-phase interleaved boost converter for pro-viding a much higher voltage gain without adopting an ex-treme large duty cycle. The proposed converter cannot only achieve high step-up voltage gain but also reduce the voltage stress of both active switches and diodes. This will allow one to choose lower voltage rating MOSFETs and diodes to reduce both switching and conduction losses. In addition, due to the charge balance of the blocking capacitor, the converter features automatic uniform current sharing characteristic of the two in-terleaved phases for voltage boosting mode without adding any extra circuitry or complex control methods. The operation prin-ciple and steady analysis as well as a comparison with other recent existing high step-up topologies are presented. Finally, a 400-W rating prototype with 25-V input and 400-V output is constructed for verifying the validity of the proposed con-verter. It is seen that the resulting experimental results indeed agree very close and show great agreement with the simulation results. Therefore, the proposed converter is very suitable for applications requiring high step-up voltage gain.

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