Estimation Of Delay And Power Analysis Of Sense Amplifiers

[1]G. Poshamallu, [2]R. Radha, [3]J. Manasa, [4]R.Pruthvi
[1]Assistant Professor, [2]Student, [3]Student, [4]Student
Mallareddy institute of technology and science

***Abstract* - Sense amplifiers plays a necessary role in CMOS memories, it is mostly used to hurry the memory read operation in a cache memory both memory access time and overall memory power consumption affects the performance of sense amplifier by use of current mode than voltage mode signal transporting technique in this we use the low resistance current signal circuits to lower the impedance level and voltage swing on extended interconnect wire, the interruption for changed power supply voltages Vdd and for altered values of bit line capacitances are specified. Results of static power and total power consumption for unlike values of Vdd are simulated and analyzed.**

***keywords* - Sense Amplifier, Voltage SA, Current SA, Cross Coupled CMOS inverter SA, Latch type voltage SA, Hybrid mode SA, Delay, Power, Static Power.**

1. INTRODUCTION

SRAM based cache is most vital element of VLSI chip. The speed and power of overall system is disserted peripheral circuit the delay in reading is the most concern in the designing of SRAM cache after latching process the current flow stops automatically. Thus, in Sense amplifier there is no dissipation of static power [3]. The delay in sensing and latching Operation is related to power dissipation. 90% of the on-chip cache the power dissipation becomes preeminent part of the total power consumption. Cross coupled CMOS inverter type is basic sense amplifier. Input lines act as output lines at the same time. For that reason, delay and power consumption are elevated. This drawback is eliminated in latch type voltage sense amplifier this drawback is a polished due to high input impedance phase [3]. Considering it's small input impedance, it's one of the most effective way to diminish sensing delay and power consumption of SRAM.

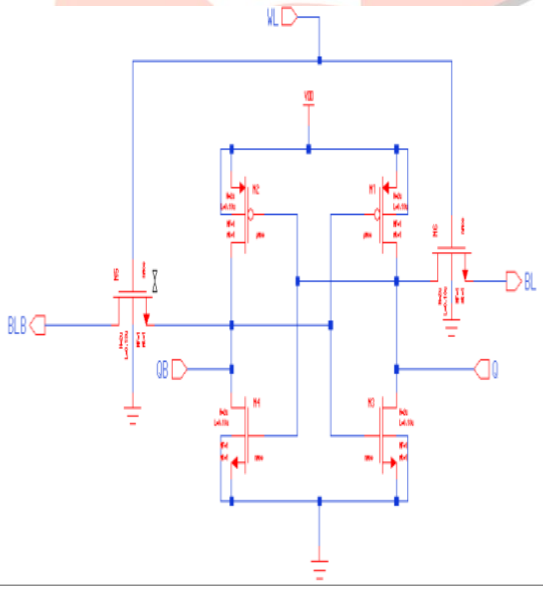

Figure 1 SRAM

SRAM

This paper encompasses the comparative study of various voltage and current sense amplifiers. The freshness of the paper is, it clarifies the purpose and gives solutions of delay and power dissipation in sense amplifiers. The paper reviews the static power dissipation for numerous sense amplifiers at transformed supply voltage. This paper evaluates delay and power dissipation of various types of sense amplifier. Implementation of altered types of sense amplifiers and their circuit diagrams are portrayed in section II. Section III explains the experimental setup for precise read operation and assessment of delay and power dissipation. Section IV compares the results of delay and overall power dissipation for analyzed sense amplifiers. Section V infers the paper.

II.IMPLEMENTATION

In read circuitry the sense amplifier is an essential part. Its main role is to sense low power signal from a bit line that characterizes data (0 or 1) gathered in memory cell. And amplifies the small voltage difference to a noticeable voltage level, in view of that data can be properly from the outside of memory cell. Considering the input signal, sense amplifier is categorized as voltage or current sense amplifier.

Voltage Sense amplifier

When a cell is read, a trivial voltage swing emerges on the bit line, amplifying the voltage sense amplifier to guide digital logic. The plainest voltage sense amplifier is cross coupled CMOS inverter latch type sense amplifier.

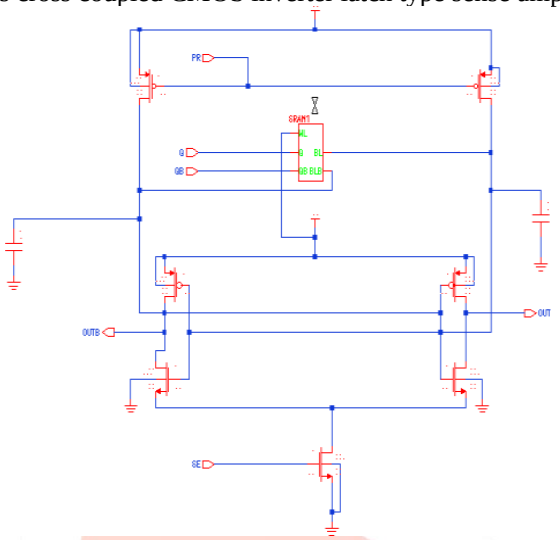

Figure 2 Cross coupled CMOS inverter SA

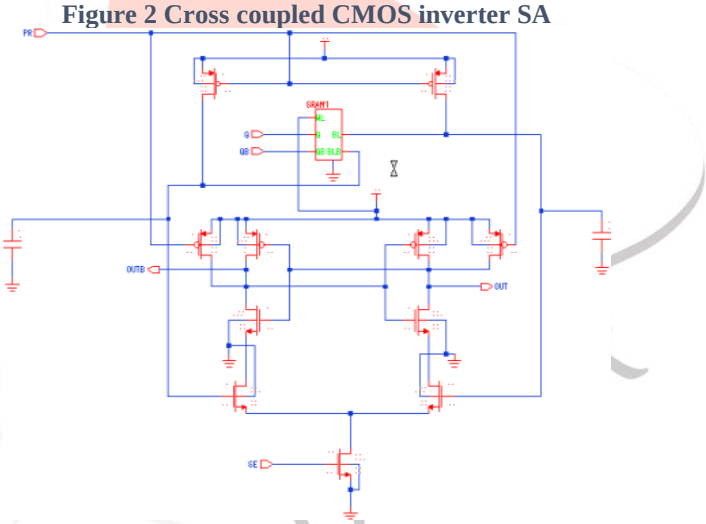

Figure 3 Latch type

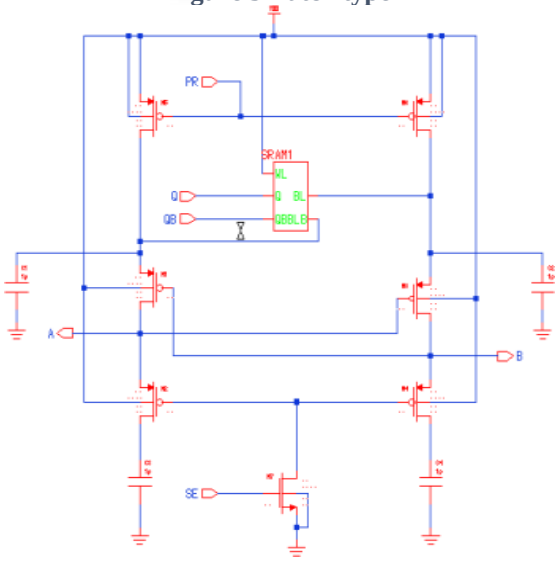

Figure 4 Basic current SA

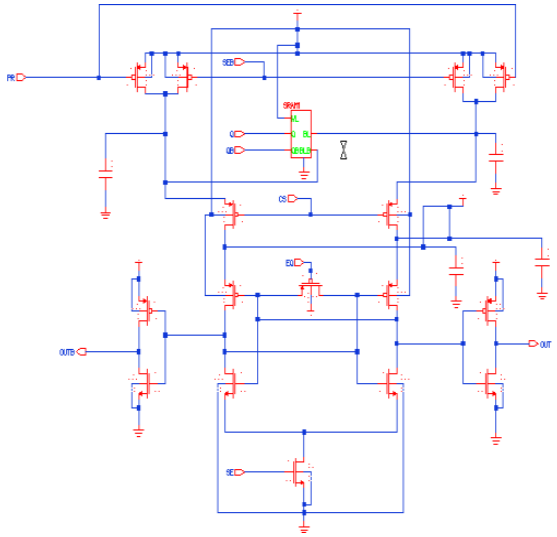

Figure 5 Hybrid mode SA

CROSS COUPLED CMOS INVERTER SA

Cross Coupled CMOS inverter SA consists of pair of CMOS cross coupled inverter (M1, M2, M3, M4). The CMOS inverter produces high gain when it is in transient region for operating.

During the receiving operation, the bit line capacitor can be discharge as a result the voltage difference is generated. If the large voltage difference is initiated, it Enables the Sense amplifier by making the SE high, depending on the input voltage, the cross coupled couple latches to one of its stable operating point. In this, the input and output are at the same mode, the bit line capacitances are directly connected to the input of cross coupled inverter.

The solution for large decision time is to separate the input and output lines by using multiplexer, pass gates. The disadvantage is eliminated in differential circuit as shown in figure 2, due to strong position feedback with a high resistive input.

Latch type voltage sense amplifier

In Fig 3, Latch type of voltage sense amplifier merges firm positive feedback with a high resistive input. Transistor M1, M2, M3, M4 acts as high gain positive feedback SA, transits M5, M6 acts as a differential amplifier, transits M7 is used to enable the SA. Whenever SE signal is high by turn on M7 therefore M5 and M6 acts as common source differential amplifier transistors M1, M2, M3 and M4 amplify the small voltage difference to full swing at output node. As input is conducted to the differential amplifier, it amplifies the tiny voltage difference of bit lines to a strong positive feedback. Once the latching process completes, turn on the sense amplifier M7 therefore no current will flow through the circuit. Henceforth, overall power dissipation will be diminished.

Current Sense Amplifier:

The slight transformation in the input is amplified by the current sense amplifier. As technology advances sub-micron, current sensing technique is much appropriate for high speed, low voltage operation and huge size memories.

Basic current sense amplifier:

Fig 4, Basic current SA consist of six pmos transistors, the sense amplifier is turned on by raising SE signal transistor M7 to high, then current flows from bit lines through a pmos transistor to the data lines which is near to ground.

The transistor M1, M4 are pmos and having equal gate to source voltages, both transistors are equal size and are in saturation. Similarly, transistors M2 and M3 also. Let the current flow over the memory cell. Thus, when sense amplifier turns on, current flowing over the sides of sense amplifier differ from current. Hence, we acquire the current sensing, so this sensing delay is not much affected to the bit lines capacitance. Consequently, different current flowing finished the data lines or differential voltages at nodes A&B. This can be further amplified in second phase.

Hybrid mode Sense Amplifier

Figure 5 displays input given as current from bit line capacitor and output is denoted as voltage acquired from cross coupled inverter. Hybrid mode sense amplifier resides of 11 PMOS and 5 NMOS. Transistors M9 and M10 is used to bond bit line and Vdd. The size is large enough to weekly connect to Vdd. Transistors M1 and M2 connects BLs to the DLs by acting as a switch. Cross coupled inverter latch is formed by PMOS M3 and M4 and NMOS M6 and M7 which is positive feedback amplifier. The bit lines and data lines to Vdd through the respective precharge circuits are kept the before read operation. During this time convert the equalization signal low to make voltages at node A and B equal.

Bit lines and data lines are remained at Vdd, in the cell where 1 Different types of analysis for delay and power dissipation are operated after correct sensing. After precharging the bit lines and output lines, the time delayed by the sense amplifier to is stored. And in the cell where 0 is present, discharge current is flown from bit line and data line to the minor voltages than Vdd.

III. EXPERIMENTAL SETUP

Experimental setup of sense amplifier is considered in two modes, one is precharging mode and other is sensing mode

Precharging Mode

Precharging is the initial course of read operation. Both the bit lines charge to Vdd in precharging mode. Sense amplifier is switched off by making SE signal low to avoid the static power dissipation. To carry the cross coupled inverter in transition as to equalize or precharge the output lines to the same voltage.

Sensing mode

The second of read operation is sensing the node voltage. The bit lines and output lines should be precharged to Vdd before sensing operation. In sensing process, the node where 0 is stored discharging current flows through it. As a final point of sensing process, it presents the data remained in the cell by reading the voltages at bit lines. Node at which 0 is present, one-bit line goes to ground and the other one remains at Vdd. Figure 6 and 7 show the reading operation of latch type voltage sense amplifier and hybrid mode sense amplifier correspondingly.

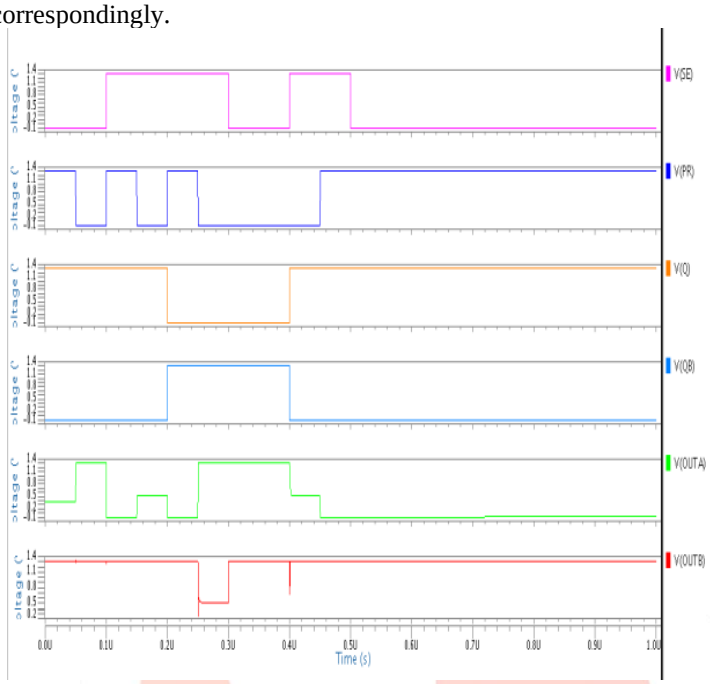

Figure 6 Reading operation in Latch type SA

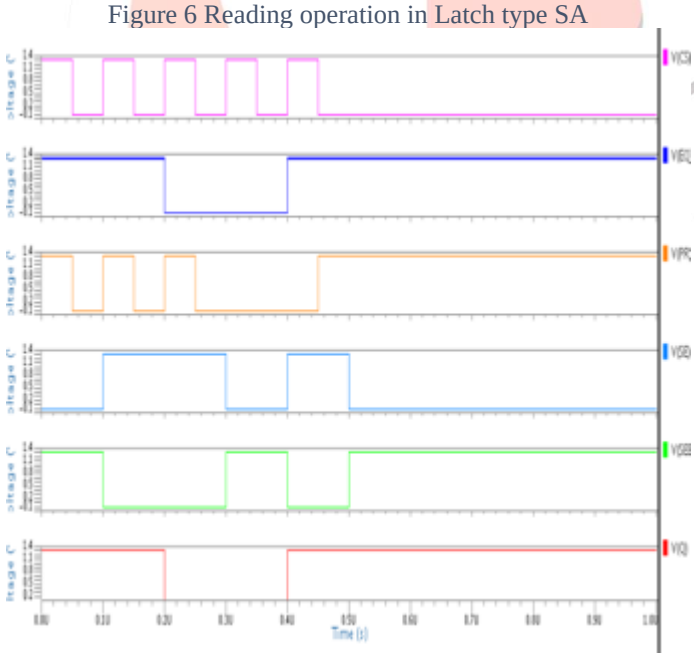

Figure 7 Reading operation of hybrid mode

give ample large voltage difference at bit line is called as delay. The different currents sense amplifiers and voltage sense amplifiers is shown in following figures. Figure 7 illustrates delay for variations in bit line capacitances. This graph shows, as capacitance increases delay also rises. The delay is time taken by bit line capacitance to discharge. The graph shows cross coupled CMOS inverter mode sense amplifier has very large delay due to same input and output node

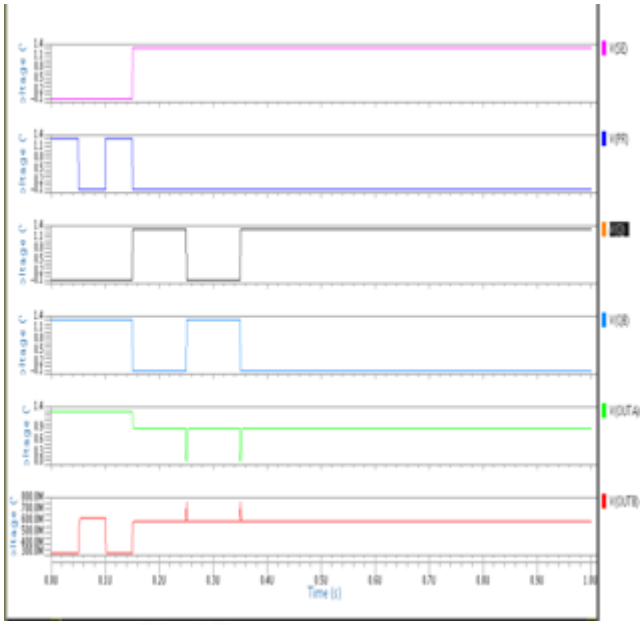

Figure 8 Reading operation of Cross Coupled CMOS inverter

Figure 8 shows delay variation due to supply voltage variation. This graph implies, as power supply increases the delay decreases. In this delay is in verse proportional to the power supply voltage.
Figure 9 shows variation static power dissipation through the circuit for variation in power supply voltage. Before the static power calculation, precharge bit line and output nodes to Vdd. Make sure sense amplifier is in off state. Then calculate static power for numerous values of supply voltage

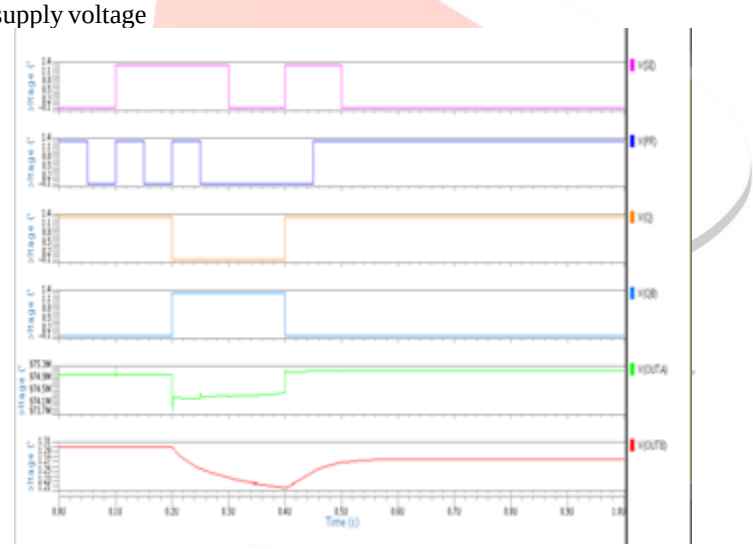

Figure 9 Reading operation of basic current sense amplifier

CONCLUSION

In cache memory Sense amplifier is an important element as its performance alters both delay in decision and total power dissipation in memory. Result shows hybrid mode sense amplifier has the most least delay and small power dissipation. Figure 7 shows delay in hybrid mode sense amplifier suitable to bit line capacitors. In cross coupled inverter sense amplifier as both input and output nodes are same, therefore, it takes large time to discharge the bit line capacitance and gives correct results.

DELAY AND TOTAL POWER COMPARISION AT 180NM

Types of SA	Bit line(ns)	Total Power dissipation	
Cross Coupled CMOS	12.620ns	202.062mw	
Latch	50.103ns	2.45mw	
Basic	50.915ns	2.068mw	
Hybri d mode	612.75ns	91.508pw	

DELAY AND TOTAL POWER COMPARASION AT 130NM

Types of SA	Bit line (nS)	Total power dissipation
Cross Coupled CMOS	100.12ns	1.172mw
Latch	50.375ns	2.705nw
Basic	50.094ns	37.63uw
Hybrid	9.238ns	2.0753nw

Accordingly, current sense amplifier has low delay in comparison to voltage sense amplifier. The hybrid mode as low transporting delay has the input is current signal. And in the output phases, the small difference is amplified immediately by the cross coupled inverter in transient area. As follows hybrid mode sense amplifier has minute delay and it turns out liberated of the bit line capacitances.

ACKNOWLEDGEMENT

Authors would like to take this opportunity to thank department of Electronics and Telecommunication, College of Engineering Pune, for providing lab and work environment. Authors express a deep sense of gratitude towards our internal examiner for providing insights, encouragement and inspiration throughout the project work.

REFERENCES

[1] E. Seevinck, P. J. V. Beers, and H. Ontrop, "Current-mode Techniques for High-Speed VLSI Circuits with Application to Current SA for CMOS SRAMs" IEEE J. Solid-State Circuits, vol. 26, no.5, pp. 525536, May 1991.

[2] R. Singh and N. Baht, "An Offset Compensation Technique for Latch Type Sense Amplifiers in High- Speed Low-Power SRAMs," IEEE Trans. VLSI Syst. Trans. Briefs, vol.12, no. 6, pp. 652657, Jun. 2004.

[3] B. Witch, T. Nirschil, and D. S. Landsiedel, "Yield and Speed Opti- mization of a Latch-type Voltage Sense Amplifier," IEEE J. Solid-State Circuit, vol. 39, no. 7, pp. 11481158, Jul. 2000.

[4] V. Gountis, K. Kristovski, and L. Yuri," New Sense Amplifier for Small- Swing CMOS Logic Circuits," IEEE Trans. Circuits and Systems II: Analog and Digital Signal Processing, Vol. 47, No. 6, pp. 573-576, June 2000.

[5] Anh-Tuan Do, Zhi-Hui Kong, Kiat-Seng Yeo, and Jeremy Yung Shern Low, "Design and Sensitivity Analysis of a New Current-Mode Sense Amplifier for Low-Power SRAM," IEEE Trans. VLSI Syst. vol. 19, no. 2, February 2011.