Design and Analysis of Radiation Hardened Latches for Nano-Scale CMOS

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Abstract - **Modern nanotechnology is advancing very fast and its operation is extensively analyzed and thus with the advancement at the level of nano-scale, the CMOS has become more sensitive to externally induced radiation which can cause induced errors called soft errors. So the tolerance to such errors is the strict requirement in the nano-scale industry. But traditional error tolerance method results in an increase in the power and area and at the same time a reduction in the performance of the circuit. This project deals with some new hardening circuits to improve performance and all other factors, these circuits are Schmitt-trigger based circuits and one circuit is used in cascode feedback loop. Schmitt–trigger based circuit gives the higher critical charge which is used as an analytical factor in the measurement of the degree of radiation hardening.**

keywords - **Critical Charge; Schmitt-Trigger; Radiation Hardening**

I. INTRODUCTION

In the modern digital world as there is a continuous advancement in nano-scale technology or the deep sub-micron technology, the IC size is shrinking to a greater extent and has reached the nanometer range. This implies a down scaling of the voltage or power supply. The reduction in supply voltage is directly affecting the transiently induced faults on these electronic chips. This gives rise to an increase in Transient Faults TFs. The direct implication is from the fact as in nano0scale devices with less supply voltages there is a reduction in the charge that is stored on the different nodes of the circuit, also there is a considerable decrease in the noise margins. The reduction in noise margin and reduction in the charges stored in internal nodes of the circuit result in more possibility of random voltage glitches on those nodes and can cause variation in voltage or current levels of the nodes from the ideal case. The probable causes of these effects can be grouped as the effects due to cross talk between the connecting lines, electromagnetic fields and interference, noise of the power supply sources, excited ambient particle like neutrons and alpha radiations. The interaction of the silicon bulk with these excited high energy particles can cause creation of minority charge particles and thus an unwanted correct is seen from drain to source. This also alters the charge stored on the internal nodes of the circuit. The problem gets severe when it comes to storage elements and the memory cells. The change in cell values thus deteriorates the integrity in the data stored. The unwanted effects caused due to radiation can be sub grouped into two classes: Single event faults/effects caused by the interaction with single particle that causes deviation from normal behavior of the circuit. The other is a cumulative effect because of prolonged exposure of the circuit to the radiation.

A. Cumulative effects

It can be divided in two categories. The Total Ionizing Dose and the Displacement Damaged Dose. The former is caused due to interaction with excited particles like electrons, alpha particles or the X-ray particles with high energies and the later is caused due to interaction with heavy mass particle like the protons and the heavy ions. The cumulative effects majorly occur when these charged, high energy particles interact with the gate oxide region for a prolonged duration and causing a permanent physical change in terms of trapping of charges and a shift in threshold voltage for the MOS device.

B. Single event effects

The effect of the charged particles on the junction or the nodes in the circuits causing a functional change in the values of those nodes for short period of time are termed as single event effects. The effect of the excited particles on these nodes can cause a sudden rise in current/voltage on some critical circuit nodes causing two kinds of errors. The soft error and the hard error.

The Soft Error is a non-destructive error as in it does not cause a permanent change or damage to the IC functionality or the physical characteristics. The Hard Error on the other hand are destructive in nature and can lead to a permanent change in IC physical structure and the functionality. A Soft error occur when the total charge generated on any node is greater than some critical charge of the node under consideration

II. CRITICAL CHARGE

The radiation hardening techniques or the fault tolerent schemes aims for a reduction in the possibilty of occurence of a Transient fault by maintaining a high critical charge Q_{crit} of those circuit nodes which are more susceptible to Transient fault. The Q_{crit} can be defined as that minimum charge that is injected by an high energy particle which hits the node and produces a node voltage value so as to cause a change in the voltage values of the dependent nodes. The Q_{crit} is dependent on the gate strength of the driving transistor of the node under consideration, and also on the capacitance of that node. The factor that can help in increasing the critical charge is an increase in the total capacitance of the node. To achieve this external capacitance can be added or the sizes os the transistor can be increased for the fan out gates. But this leads in power and area constraints to increase thus putting a limit.

Various schemes to increase this critical charge without much trade off with power or area is considered in this paper. A comparative analysis is made between various radiations hardened latches using different topologies. This paper work is organized in following manner. In Section 1, we gave some introduction about the general fault schemes and the causes for the same. Section 2, Analysis and problem formulation of critical charge was done. The critical charge definition and the existing methodologies to increase Q_{crit} had checked. Section 3 focuses on different topologies for radiation hardened latches and their description. In Section 4, we compare the performances of all the latches using a performance metric Q_{PAR}. Section 5 finally concludes with the general observations.

III. LATCH DESIGNS

A reference latch is taken into consideration and four other latches are compared. The latches differ in terms of the feedback used. For a fair comparison the frequencies for the clock and the input is kept constant. The transistor sizing is matched for all the circuits with similar properties.

A. The Reference latch

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The Fig. 1 is a widely used generalized latch topology, This circuit will be used as a reference latch for this paper. The input is denoted by D, The signals CLK and NCLK are clock and the compliment clock signals, the internal nodes are

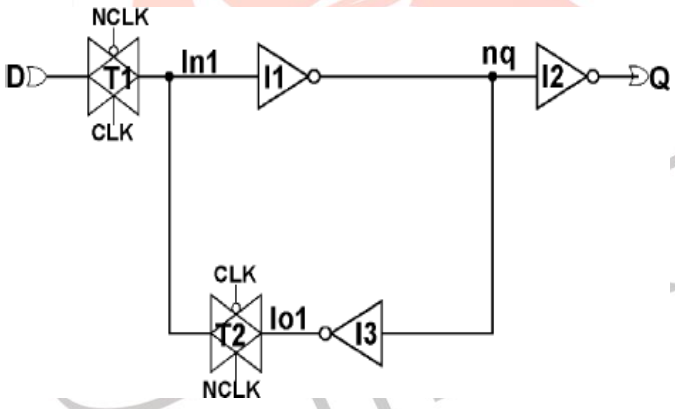


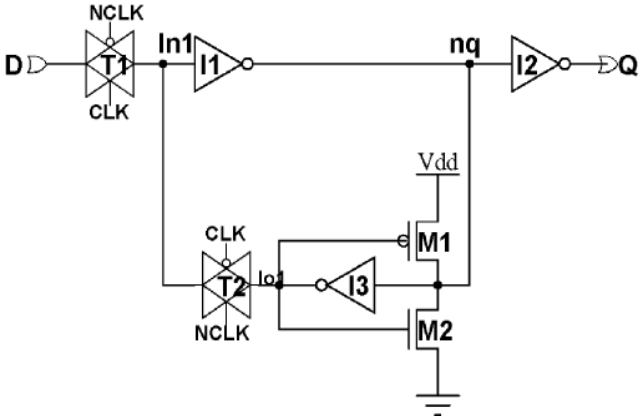
Fig. 1 The Reference latch

denoted by ln1, nq and lo1 and the output node is the Q. On inspection it is found that only those nodes should be taken into consideration where the critical charge is as minimum as this node is affected more by the same amount of radiation as compared to other nodes. The literature survey shows that ln1 node is the critical node having the least critical charge and the value being almost tenth factor of the charges on other nodes.

B. Schmitt trigger-based hardening latch

In this latch the transistor M1, M2 are used in addition to our reference latch for the functionality of the Schmitt trigger. Thus the total gate-capacitance at the node ln1 for this circuit gets increased, and in turn it increases the critical charge for node, ln1. The variations can be done in the feedback loop to effectively increase the gate capacitance and thus the critical charge. The below mentioned schematics are proposed with better critical charge.

Fig. 2 Schmitt trigger-based hardening latch



C. Modified SEM-Latch

The mentioned Schmitt trigger configuration used for the SEM latch is shown in the Fig. 2. The design in Fig. 2 can be used to mask a transient pulse arriving on the input node that is D. Thus during high phase of the clock the Schmitt-trigger suppresses generated glitches on the node D. Fig. 3 shows modification in the SEM latch that provides some improvement in the value of Q_{crit}-critical charge. The addition of the Schmitt-trigger effect using transistors M1, M2 and inverters I4 and I5 is used for increasing the critical charge.

Further modifications are done to get a better performance of the circuit. Also the power, Area and Critical charge constraints are used in the proposed circuits so as to have a better comparison of the latches. In accordance with the reference latch shown in Fig. 1, node ln1 in both SEM latch and the modified SEM latch are connected to inverter.

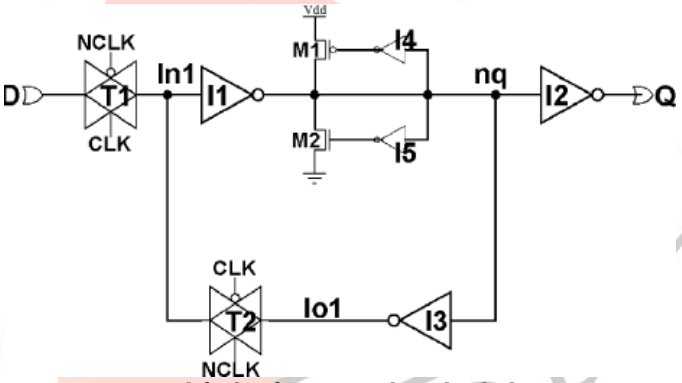


Fig. 3: Modified soft error masking latch design .

D. Proposed Schmitt- trigger-based latch

The advanced hardened latch, Schmitt-trigger ST latch is proposed in the Fig. 4. In this design the latch critical node ln1 forms a Schmitt-trigger which uses transistors M1,M2,M3,M4,M5,M6. The functioning of the circuits can be given as follows. For low states of node In1, the node nq remains high and the node Int2 gets charged while the transistor M6 is in ON state. Suppose now a transient faults on the In1 node switches from low state to high state then for a change in state of the node nq, charge stored on node Int2 must be discharged. Same phenomenon can be explained for negative polarity pulse hitting on node In1. Thus we can see that this latch proves to be a better tolerant for soft errors and is robust by the virtue of charges on node Int1 and node Int2. The care should be taken on the sizing of the transistors useed in Schmitt-trigger as the hysteresis width lines can reduce the speed performance of the latch. For a low clock signal and high NCLK signal, the feedback patch holds the data so as the soft errors is not affected and proves to be more tolerent.

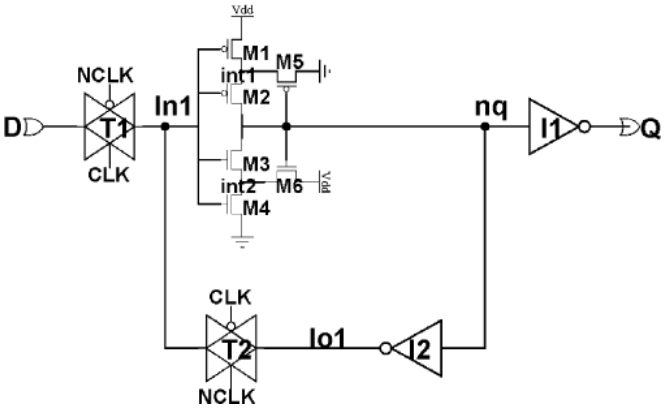


Fig. 4: Proposed Schmitt trigger-based latch.

E. Cascode ST latch

A slight modification is done in feedback path of Fig 4, and Fig 5 is proposed with this modification in [2]. In Fig 4 it is seen that the feedback path uses a Inverter l2 along with clock controlled (T2) Transmission gate in series, the modification for Fig 5 includes a clocked inverter where both the latches work the same and use the cascade circuit configuration. The difference in the two circuits is from existing metastable stable during the data retaining phase of the latch. In [?] it is shown that using a cascode configuration increases the capabilities of the latch for exiting the metastable state as compared to the configuration using the transmission gate. This is achieved mainly by removing the TG which causes signal degradation because of the Miller effect when applied for small signal amplifiers. At high and low clock pulses the functionality of the two latches in Fig 4 and Fig 5 remains the same. The power, area and the delay measurements of the two latches are approximately of comparable values. A slighlty better critical charge is observed in the Fig 5 configuration.

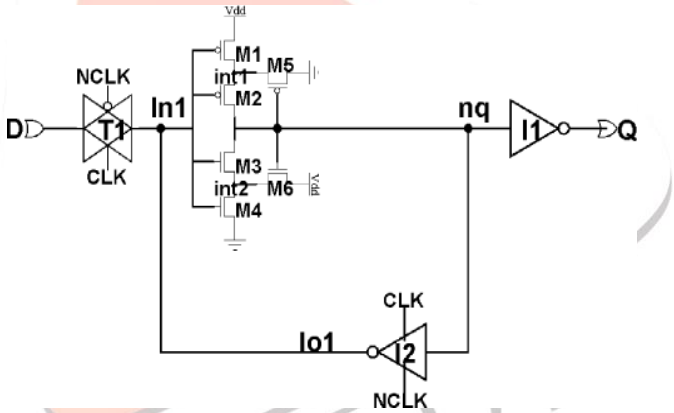


Fig. 5: Cascode feedback Schmitt-trigger latch

F. HLR Latch

A new HLR latch denoting a High performance, Low cost and robust latch is proposed in [4]. The circuit is shown in Fig 6. The operation of this latch can be elaborated as follows. During the ON phase of TG1, TG2 and TG3, latch will be in transparent mode. The input D will pass to the output Q via gates TG1 through TG3. The node d1 and node d2 are connected to the input D via gates TG1 and TG3 respectively. The node d1 drives the node d1b through the inverter I1. Similarly node d2 drives the node d2b through the inverter I3. During this phase the Inverters I2 and I4 remain OFF using the clock signal thus avoiding any possibility of contention on internal nodes d1 and d2. The output stage consists of transistors M1 to M6 also remains OFF during this phase using clock signal and avoids the contention on Q.

During the latch mode the transistors of gates TG1 to TG3 are in OFF state. Thus the nodes d1, d2 and node Q gets disconnect from input. During this stage output -stage consisting of transistors M1 - M6 are ON along with the inverters l2 and l4. Inverters l2 and l4 maintain the values at node d2 and node d2b which implies that voltage value on node Q is maintained by the node d2 and node d2b. That suggests if any transient faults generates on any internal node then the output voltage value can be preserved.

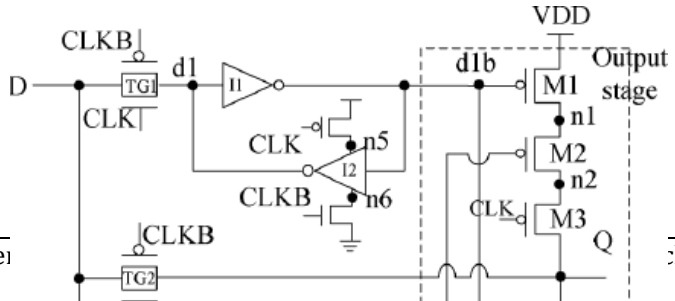


Fig. 6: The HLR-latch

The latch mode operation where clock signal is low we can evaluate using two cases when a TF occurs considering node d1. In the first case: 1) If Q = 1, then nodes d1b and d2b will be at low value 0, Transistors M5, M6 are OFF and M1, M2 are ON. In second case: 2) If Q = 0, then nodes d1b and d2b will be at high value 1, Transistors M5, M6 are ON and M1, M2 are OFF. Considering case 1: Now if d1b changes to 1 due to occurrence of TF at d1, then M1 will be turned OFF and transistor M5 will be turned ON. Thus the path between Q and V_{dd} is cut off and can cause Q to go in high-impedance state. But due to cut off path the previous value of Q gets unchanged thus resisting to TF. Similarly case 2: If d1b changes to 0 due to occurrence of TF at d2, which turns ON transistor M1 and turns OFF transistor M5. Thus the path between Q and Gnd is cut off and can cause Q to go in high- impedance state. But due to cut off path the previous value of Q gets unchanged and is TF tolerant.

Consider TF is generated on node from any n1 to n4, then a glitch can be generated on node Q as the node Q is driven using transistors M1 - M6. Similarly if a TF generates on node n6 or node n5, then a glitch can be generated on node d1. Lastly, TF generates on node n8 or n7, then a glitch can be generated on node d2. All these cases have similar interpretations as the above two cases finally providing a better mechanism for fault tolerance against the TFs.

IV. FIGURE OF MERIT

The metric for evaluating the performance of the latch in terms of the radiation hardening property along with other constraints like power, area and delay is used in [2]. The QPAR is defined in terms of Charge-Q, and the Power delay product + Area. The mathematical expression is given as:

$$QPAR = \frac{\text{Critical Charge } (Q_{crit})}{\text{Power} * (T_{setup} \quad D_{C\ Q}) * Area}$$

The comparison table for all the latches is given in below:

Table I: Comparison Table

Latch	Reference Latch	SEM-Latch	Modified SEM-Latch	ST-Latch	Cascode ST-latch	HRL Latch
Q_{crit} (fC)	14.6	15.6	16.4	18	16.8	16e5
Power (μW)	4.0	7.403	6.968	7.513	8.839	1.5e5
T_{setup} (ns)	0.1	0.1	0.1	0.1	0.1	0.1
D_{CQ} (ns)	0.06	0.05	0.118	0.258	0.218	0.06
D(ns)	5.7	5.7	5.7	5.7	5.7	5.7
Area	29.5	33.9	44.15	36.72	50.72	53.62
Q_{par}	7.89e5	8.14e5	2.445e5	2.63e5	8.78e5	1.3e7

V. CONCLUSION

All the Latches have been compared on the basis of Critical charge and QPAR. For fair comparison the Input and Clock frequencies have been kept same. All latches were simulated in cadence using 90nm technology. A supply voltage of 1.2 V was used. Comparison shows that the HLR latch show better performance with respect to mentioned figure of merit- QPAR. For finding the final value, the HLR latch is given a very high current for finding the exact values. The HLR latch is approximately radiation hardened to all possible transient effects within a digital domain, thus the HLR latch have highest tolerance to soft errors.

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