High Gain DC-DC Boost Converter with Coupled Inductor for PV Systems

1Parth R. Rana, 2Dr. Bhavin J. Shah
1M.E. Student Scholar, 2Associate Professor
L. D. College of Engineering, Ahmedabad

***Abstract* - This Paper presents the design and analysis of a high-voltage gain dc–dc converter for photovoltaic (PV) systems. The output voltage of the renewable energy sources like photovoltaic system and fuel cell is low. So it is necessary to use dc-dc boost converter. In this work, a new boost dc-dc converter by using coupled inductor is proposed. The proposed converter achieves extremely large voltage conversion ratio with appropriate duty cycle and reduction of voltage stress on the power devices. A passive clamp network around the primary inductor ensures the recovery of energy trapped in the leakage inductance, leading to drastic improvement in the voltage gain and efficiency of the system. This passive clamp circuit reduces the voltage stress on the switch. These characteristics make it possible to design a compact circuit with high static gain and high efficiency for industry applications. This paper proposes a new converter strategy with closed loop control action. With the help of closed loop system we will get constant output voltage even if the output of PV panel is changing. The operating principles of the proposed converter is discussed in detail. At last, the simulation of the dc-dc converter is performed in MATLAB/Simulink for open loop system as well as for the closed loop system.**

***keywords* - Coupled Inductor, DC, Voltage Stress, Voltage gain**

I. INTRODUCTION

Demand for clean and sustainable energy sources has dramatically increased during the past few years with increasing energy demand and environmental concerns. Since long time ago, fossil fuels have served as the major source of generating electrical energy. However, environmental consequences of these resources tends to utilize energy from non-conventional sources such as wind and solar. Photovoltaic systems (PV) will be an ideal choice for alleviating the aforementioned problems in this regard. Output voltages of the PV modules are variable because of change of temperature and irradiation levels. As a result, the low variable voltage of these clean energy technologies requires high voltage gain dc-dc converters [2]. Traditional energy sources, such as fossil fuels and natural gas, will only last for decades at the current rate of rising energy demand. In light of the emissions caused by conventional energy sources, the planet faces a major problem in the form of an energy scarcity crisis in the near future. Solar energy and wind power are currently being considered to construct the potential energy environment, and the use of ostensibly renewable energy is a significant solution to solving the issue of energy scarcity. Developing more clean, affordable, and renewable energy options has become a hot topic in industry and academia around the world [6]. According to the world global energy system in the current years our world is experiencing electric power crises as a result of high demand of energy consumptions [1]. This is caused due to the fast diminishing of fossil-fuel sited convectional power supply systems and the rapid increase of electric energy based technology advancement. Therefore, significant researches have been developed to solve this issue. The possible feasible solutions are to develop an effective renewable power generations, advanced power conversion control systems and enhancement the efficiency of current power generation. Even though, a lot of power converters have been developed, still an improvement is required in the existing converters due to their low efficiency, high cost, low switching frequency and low voltage gain [4]. For example, renewable energies like PV systems, wind turbine and full-cell generating low voltages need a high voltage converting device before inverting to AC source connected to the main grid of the system. Because, these types of energy sources are clean, more feasible and practically accepted their application is more fame through worldwide.

Many non-isolated topologies have been researched to achieve a high conversion ratio and avoid operating at extremely high-duty cycle. These converters include the switched-capacitor types [10], [11], switched-inductor types [12], [13], the voltage-doubler circuits [15], [16], the voltage-lift types [14], and the capacitor–diode voltage multiplier. All of them can present higher voltage gain than the conventional boost converter. However, more switched-capacitor or switched-inductor stages will be necessary for an extremely large conversion ratio, resulting in higher cost and complex circuit. The quadratic boost converter using a single active switch is another interesting topology for extending the voltage gain, where the voltage conversion ratio is given as a quadratic function of the duty ratio. However, the voltage gain of this converter is moderate since the output voltage level is determined only by the duty cycle. Moreover, if the components used are ideal ones, the voltage stress of the active switch is equal to the output voltage. Thus, in high output voltage applications, a high-voltage rating switch should be selected. In [7], an improved quadratic boost converter using a coupled inductor and voltage-lift

techniques is presented, and the authors suggest how to optimal coupling coefficient of the coupled inductor for low input current ripple.

In this paper, a novel single switch dc–dc converter with high voltage gain is presented. The features of the proposed converter are as follows: 1) the voltage gain is efficiently increased by a coupled inductor and the secondary winding of the coupled inductor is inserted into a diode-capacitor for further extending the voltage gain dramatically; 2) a passive clamped circuit is connected to the primary winding of the coupled inductor to clamp the voltage across the active switch to lower voltage level. As a result, the power devices with low voltage rating and low on-state resistance R_{DS} (ON) can be selected. On the other hand, this diode–capacitor circuit is useful to increase voltage conversion ratio; 3) the leakage inductance energy of coupled inductor can be recycled, improving the efficiency; and 4) the potential resonance between the leakage inductance and the junction capacitor of output diode may be cancelled.

II. OPERATIONAL PRINCIPLE OF THE PROPOSED CONVERTER

Fig. 1(a) shows the circuit structure of the proposed converter, which consists of an active switch Q, an input inductor L_1 and a coupled inductor T_1, diodes D_1, D_2, and D_O, a storage energy capacitor C_1 and a output capacitor C_O, a clamped circuit including diode D_3 and capacitor C_2, an extended voltage doubler cell comprising regeneration diode D_r and capacitor C_3, and the secondary side of the coupled inductor. The simplified equivalent circuit of the proposed converter is shown in Fig. 4.1(b). The dual-winding coupled inductor is modeled as an ideal transformer with a turn ratio N (n2 /n1), a parallel magnetizing inductance L_m, and primary and secondary leakage inductance L_{k1} and L_{k2}.

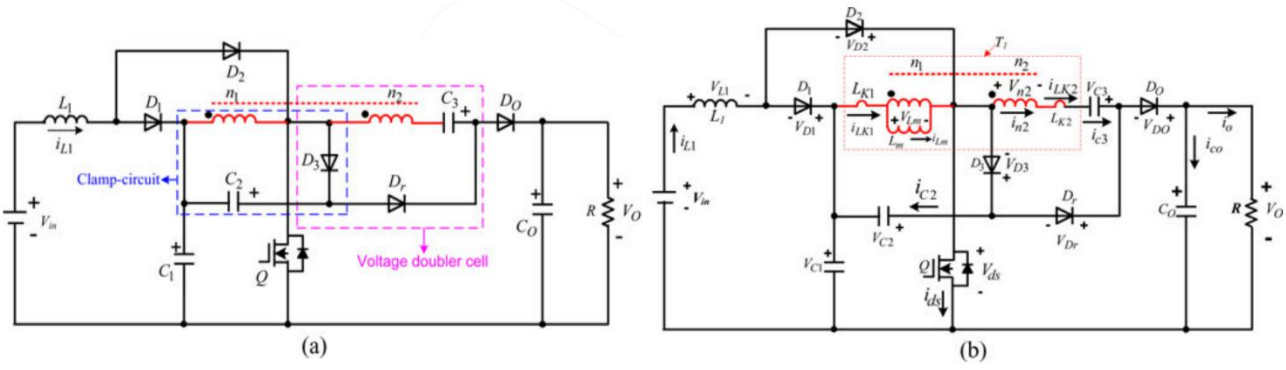

Fig. 1. Circuit configuration of proposed converter

In order to simplify the circuit analysis of the converter, some assumptions are as follows:

1) the input inductance L_1 is assumed to be large enough so that i_{L1} is continuous; every capacitor is sufficiently large, and the voltage across each capacitor is considered to be constant during one switching period;
2) all components are ideal except the leakage inductance of the coupled inductor;
3) Both inductor currents i_{L1} and i_{Lm} are operated in continuous conduction mode, which is expressed as C-CCM; the inductor current i_{L1} is operated in continuous conduction mode, but the current i_{Lm} of the coupled inductor is operated in discontinuous conduction mode, which is called C-DCM.

A. C-CCM

Based on the aforementioned assumption, some key waveforms under C-CCM operation in one switching period is shown in Fig. 2. The operating stages are described as follows:

Stage 1 [$t_0 - t_1$]: The switch Q is conducting at $t = t_0$. Diodes D_1, D_3, and D_o are reverse-biased by V_{C1} , $V_{C1} + V_{C2}$ and $V_o - V_{C1} - V_{C2}$, respectively. Only Diodes D_2 and D_r are turned ON. Fig. 3(a) shows the current-flow path. The dc source V_{in} energy is transferred to the inductor L_1 through D_2 and Q. Therefore, the current i_{L1} is increasing linearly. The primary voltage of the coupled inductor including magnetizing inductor Lm and leakage L_{k1} is $V_{C1}$and the capacitor C_1 is discharging its energy to the magnetizing inductor L_m and primary leakage inductor L_{k1} through Q. Then currents i_{D2}, i_{Lm}, and i_{k1} are increasing. Meanwhile, the energy stored in C_2 and C_1 is released to C_3 through D_r. The load R energy is supplied by the output capacitor C_o. This stage ends at $t = t_1$.

Stage 2 [$t_1 - t_2$]: In this transition interval, Fig. 3(b) depicts the current-flow path of this stage. Once Q is turned OFF at $t = t_1$, the current through Q is forced to flow through D_3 . At the same time, the energy stored in inductor L_1 flows through

diode D_1 to charge capacitor C_1 instantaneously and the current i_{L1} declines linearly. Thus, the diode D_2 is reverse biased by V_{C2} . The diode D_o is still reverse biased by $V_o - V_{C1} - V_{C2}$. The energy stored in inductor L_{k1} flows through diode D_3 to charge capacitor C_2. Therefore, the energy stored in L_{k1} is recycled to C_2. The i_{Lk2} keeps the same current direction for charging capacitor C_3 through diode D_3 and regeneration-diode D_r . The voltage stress across Q is the summation of V_{C1} and V_{C2}. The load energy is supplied by the output capacitors C_o . This stage ends when i_{Lk2} reaches zero at $t = t_2$.

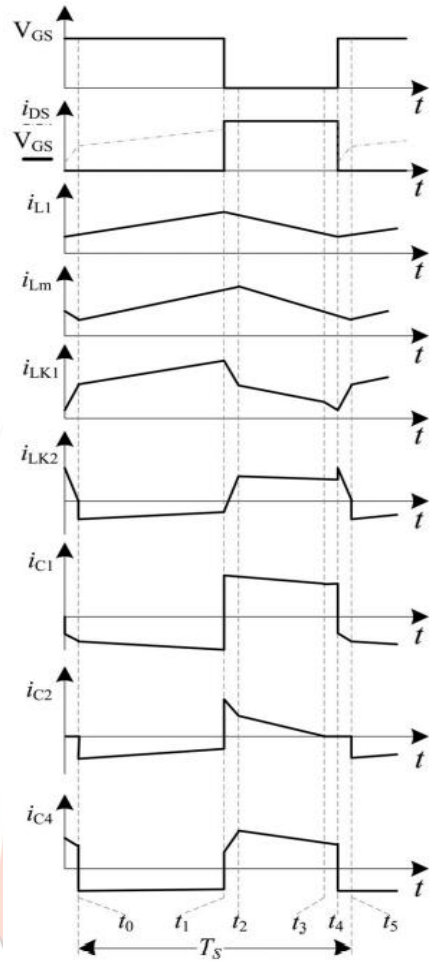

Fig. 2. The key waveforms of the proposed converter at C-CCM operation

Stage 3 [$t_2 - t_3$]: During this transition interval, switch Q remains OFF. Since i_{Lk2} reaches zero at $t = t_2$, V_{C2} is reflected to the secondary side of coupled inductor T_1 ; thus, regeneration-diode D_r is blocked by $V_{C3} + NV_{C2}$. Meanwhile, the diode D_o starts to conduct. Fig. 3(c) depicts the current-flow path of this stage. The inductance L_1 is still releasing its energy to the capacitor C_1 . Thus, the current i_{L1} still declines linearly. The energy stored in L_{k1} and L_m is released to C_2 . Moreover, the energy stored in L_m is released to the output via n_2 and C_3 . The leakage inductor energy can thus be recycled, and the voltage stress of the main switch is clamped to the summation of V_{C1} and V_{C2} . This stage ends when current $i_{Lk1} = i_{Lk2}$, thus the current $i_{C2} = 0$ at $t = t_3$.

Stage 4 [$t_3 - t_4$]: During this time interval, the switch Q, diodes D_2 and D_r is still turned OFF. Since i_{C2} reaches zero at $t = t_3$, the entire current of i_{Lk1} flows through D_3 is blocked. The current-flow path of this mode is shown in Fig. 3(d). The energy stored in an inductor L_1 flows through diode D_1 to charge capacitor C_1 continually, so the current i_{L1} is decreasing linearly. The dc source V_{in} , L_1 , L_m, L_{k1}, the winding n_2 , L_{k2} and V_{C3} are series connected to discharge their energy to capacitor Co and load R. This stage ends when the switch Q is turned ON at $t = t_4$.

Stage 5 [$t_4 - t_5$]: The main switch Q is turned ON at t_4. During this transition interval, diodes D_1, D_3 and D_r are reverse-biased by V_{C1} , $V_{C1} + V_{C2}$ and $V_o - V_{C1} - V_{C2}$, respectively. Since the currents i_{L1} and i_{Lm} are continuous, only diodes D_2 and D_o are conducting. The current-flow path is shown in Fig. 3(e). The inductance L_1 is charged by input voltage V_{in} , and the

current i_{L1} increases almost in a linear way. The blocking voltages V_{C1} is applied on magnetizing inductor L_m and primary-side leakage L_{k1}, so the current i_{Lk1} of the coupled inductor is increased rapidly. Meanwhile, the magnetizing inductor L_m keeps on transferring its energy through the secondary winding to the output capacitor C_o and load R. At the same time, the energy stored in C_3 is discharged to the output. Once the increasing i_{Lk1} equals the decreasing current iLm and the secondary leakage inductor current i_{k2} declines to zero at $t = t_5$, this stage ends.

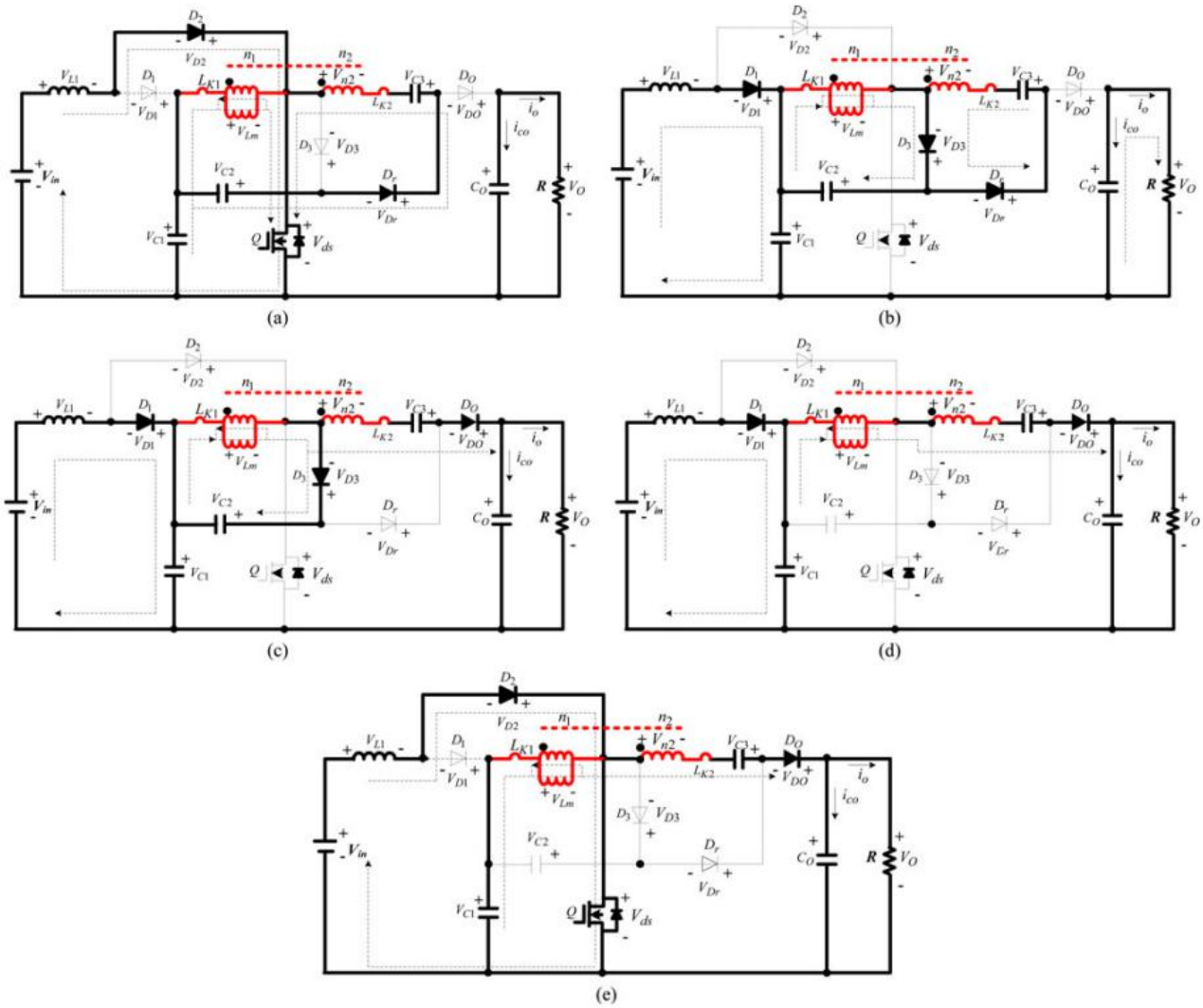

Fig. 3. Equivalent circuits of five operating stages during one switching period at C-CCM operation.

B. C-DCM

To simplify the C-DCM analysis, all leakage inductances of the coupled inductor are neglected. The coupled inductor is modeled as a magnetizing inductor Lm and an ideal transformer. The key waveforms of the proposed converter are shown in Fig. 4. There are four main stages during one switching cycle.

Stage 1 [$t_0 - t_1$]: During this time interval, Q is turned ON. Diodes D_2 and D_r are conducted but diodes D_1, D_3, and D_o are blocked by V_{C1} , $V_{C1} + V_{C2}$, and $V_o - V_{C1} - V_{C2}$, respectively. The current-flow path is shown in Fig. 5(a). The inductance L_1 is charged by input voltage V_{in} ; thus, the current i_{L1} increases linearly. The energy from capacitor C_1 transfers to magnetizing L_m and current i_{Lm} increases linearly. Meanwhile, capacitor C_3 is charged through the secondary winding coil n_2 by capacitors C_1 and C_2. The output capacitor C_o provides its energy to load R. The clamped diode D_3 is biased forward when the main switch Q is turned OFF at $t = t_1$, and this stage ends.

Stage 2 [$t_1 - t_2$]: At $t = t_1$, the switch Q is turned OFF, resulting in a current commutation between the switch Q and diode D_3 immediately. During this transition time interval, diodes D_2 and D_r are turned OFF because they are respectively anti biased by V_{C2}, and $V_o - V_{C1} - V_{C2}$, and other diodes are conducting. The current-flow path is shown in Fig. 5(b). The dc sources V_{in}, is series-connected with inductor L_1 and transfer their energies to the capacitor C_1 through D_1. The capacitors C_2 is charged by the magnetizing inductor L_m via D_3. Similarly, the dc source V_{in}, inductor L_1 , magnetizing inductor L_m and capacitor C_3 are series

connected to transfer their energy to capacitor C_o and load R. This stage ends when the rising current i_{C3} equals to current i_{Lm} at $t = t_2$. At the same instant, the diode D_3 is reverse biased at $t = t_2$.

Stage 3 [$t_2 - t_3$]: During this time interval, the switch Q, D_2 and D_r remain turned OFF. The diodes D_1 and D_o are still turned ON. Since i_{C2} reaches zero at t_2, the coupled inductor transfers energy to the output, and diode D_3 is also blocked. The current-flow path is shown in Fig. 5(c). The dc source V_{in} and the input inductor L_1 are still connected serially to charge capacitor C_1. Thus, the current i_{L1} continues to decrease. Meantime, the primary and secondary sides of doubled-inductor are serially connected, and serially connected with V_{C3}, delivering their energy to the output capacitor C_o and load R. This stage ends when the current i_{Lm} reduces to zero at $t = t_3$.

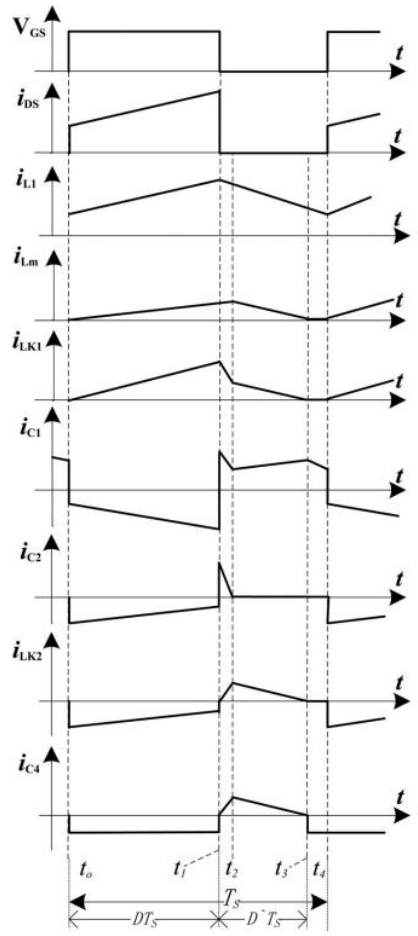

Fig. 4. The key waveforms of the proposed converter at C-DCM operation.

Stage 4 [$t_3 - t_4$]: During this transition time interval, the switch Q and the diode D_2 is still turned OFF. Meanwhile, the primary and secondary currents of the coupled inductor have run dry at t_3 . Therefore, the diode D_3 is still blocked by $V_{C1} + V_{C2}$, and only diode D_1 is conducting for continuous i_{L1} . The current-flow path is shown in Fig. 5(d). The capacitor C_1 is still charged by the energy stored in L_1 and dc sources V_{in} . Since the energy stored in L_m is empty, the energy stored in C_o is discharged to load R. This stage ends when Q is turned ON at $t = t_4$, which is the beginning of the next switching period.

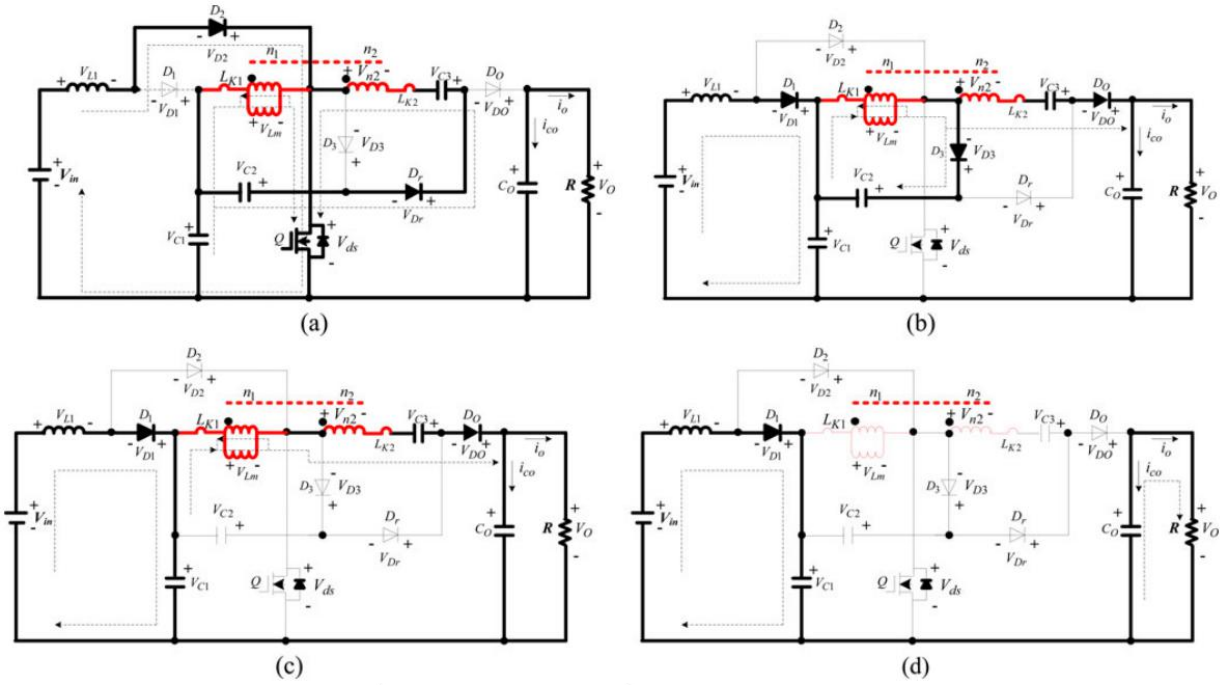

Fig. 5. Equivalent circuits of four operating stages during one switching period at DCM operation.

III. STEADY-STATE PERFORMANCE ANALYSIS OF THE PROPOSED CONVERTER

C-CCM Operating Conduction

To simplify the analysis, the leakage inductances of the coupled inductor are neglected in the steady-state analysis. Also, the losses of the power devices are not considered. Only stages 1 and 3 are considered for C-CCM operation because the time durations of stages 2, 4, and 5 are short significantly. At stage1, the main switch Q is turned ON, the inductor L_1 is charged by the input dc source V_{in}, and the magnetizing inductor L_m is charged by the voltage across C_1 . The following equations can be written from Fig. 3(a):

$$V_{L1} = V_{in} \tag{1}$$

$$V_{Lm} = V_{C1} \tag{2}$$

And the voltage of the switched capacitor C_3 can be expressed by,

$$V_{C3} = NV_{C1} + V_{C1} + V_{C2} \tag{3}$$

During stage 3, the main switch Q is in the OFF state, the inductor L_1 and magnetizing inductor L_m are discharged, respectively. The voltages across the inductor L_1 and L_m can be obtained by,

$$V_{L1} = V_{in} - V_{C1} \tag{4}$$

$$V_{Lm} = - V_{C2} \tag{5}$$

$$V_o = V_{C1} + (N + 1) V_{C2} + V_{C3} \tag{6}$$

Using the inductor volt-second balance principle to the inductor L_1 and magnetizing inductor L_m , the following equations can be expressed as:

$$\int_0^{DT_s} V_{in}\, dt + \int_{DT_s}^{T_s} (V_{in} - V_{C1})\, dt = 0 \tag{7}$$

$$\int_0^{DT_s} V_{C1}\, dt + \int_{DT_s}^{T_s} (- V_{C2})\, dt = 0 \tag{8}$$

From (1)–(8), the voltages across capacitors C_1, C_2, and C_3 are derived as follows:

$$V_{C1} = \frac{V_{in}}{1 - D} = \frac{(1 - D) V_O}{2 + N} \tag{9}$$

$$V_{C2} = \frac{D.V_{in}}{(1-D)^2} = \frac{DV_O}{2+N} \tag{10}$$

$$V_{C3} = \frac{(N+1-DN)V_{in}}{(1-D)^2} = \frac{(N+1-DN)V_O}{2+N} \tag{11}$$

Substituting (9)–(11) into (6), the dc voltage gain M_{C-CCM} is obtained as

$$M_{C-CCM} = \frac{V_O}{V_{in}} = \frac{(2+N)}{(1-D)^2} \tag{12}$$

From the above equations, it can be concluded that the voltage gain of the proposed converter is determined by the turn ratio of the coupled inductor and the duty ratio of the main switches.
According to the description of the operating stages and neglecting the voltage ripple on the clamp capacitor, the maximum voltage stress of the main switch can be derived by,

$$V_{stress-Q} = \frac{V_o}{2+N} \tag{13}$$

In the conventional quadratic boost converter, the voltage stress of the main switch always equals to the output voltage. The main switch voltage stress of reference [2] is determined by duty cycle and the turn ratio of the coupled inductor, which is far lower than the output voltage with increasing duty ratio. Fortunately, the voltage stress of the main switch in the proposed converter is only determined by the turn ratio of the coupled inductor and the output voltage. One can see that the voltage stress of the switch decreases sharply with increasing turns ratio. Thus, the high-performance active switch can be used here to improve the efficiency.
The voltage stress on the diodes are given by

$$V_{stress-D_1} = \frac{V_{in}}{1-D} = \frac{(1-D)}{(2+N)}.V_o \tag{14}$$

$$V_{stress-D_2} = \frac{D}{(1-D)^2}.V_{in} = \frac{D}{(2+N)}.V_o \tag{15}$$

$$V_{stress-D_3} = \frac{V_{in}}{(1-D)^2} = \frac{1}{(2+N)}.V_o \tag{16}$$

$$V_{stress-D_o} = \frac{(1+N)}{(1-D)^2}.V_{in} = \frac{(1+N)}{(2+N)}.V_o \tag{17}$$

$$V_{stress-D_2} = \frac{(1+N)}{(1-D)^2}.V_{in} = \frac{(1+N)}{(2+N)}.V_o \tag{18}$$

In terms of the operating principles, the current ripples on the input inductor and magnetizing inductor are expressed as

$$\Delta I_{L1} = \frac{DT_s.V_{in}}{L_1} \tag{19}$$

$$\Delta I_{Lm} \approx \frac{DT_s.V_{C1}}{L_m} \tag{20}$$

IV. MATLAB MODELLING AND SIMULATION RESULTS

In order to evaluate the performance, simulation is carried out in two different cases 1) Implementation of Proposed Converter with constant DC Sources operated in CCM mode Operating in Open Loop System. 2) Implementation of Proposed Converter Operating in Closed Loop System. The Parameters of the converter are described in Table 1.

Table 1 Components

Components	Parameters

Switching Frequency (f_s)	40 kHz
Load	500 W
Input Inductor (L_1)	60μH
Magnetizing Inductance (L_m)	200.1μH
Turns ratio of Coupled inductor (N)	11/7
C_1, C_o	470μF
C_2, C_3	47μF

A. Implementation of Proposed Converter with constant DC Source operated in CCM mode Operating in Open Loop System

For the purpose of topology testing, all the components are ideal except for the Coupled Inductor, whose magnetizing inductance is still taken into consideration. A pulse generator is used for generation of 40 KHz frequency. 24 V is given as an input to the converter. MOSFET is used as a switching device in the Simulink model. Calculation for the voltage gain is shown below:

$$M_{C-CCM} = \frac{V_O}{V_{in}} = \frac{(2 + N)}{(1 - D)^2}$$

$$M = 14.28$$

The input voltage (Vin) is 24 volts, as gain is 14.28, the output voltage (Vo) should be around 340 volts from the theoretical analysis.

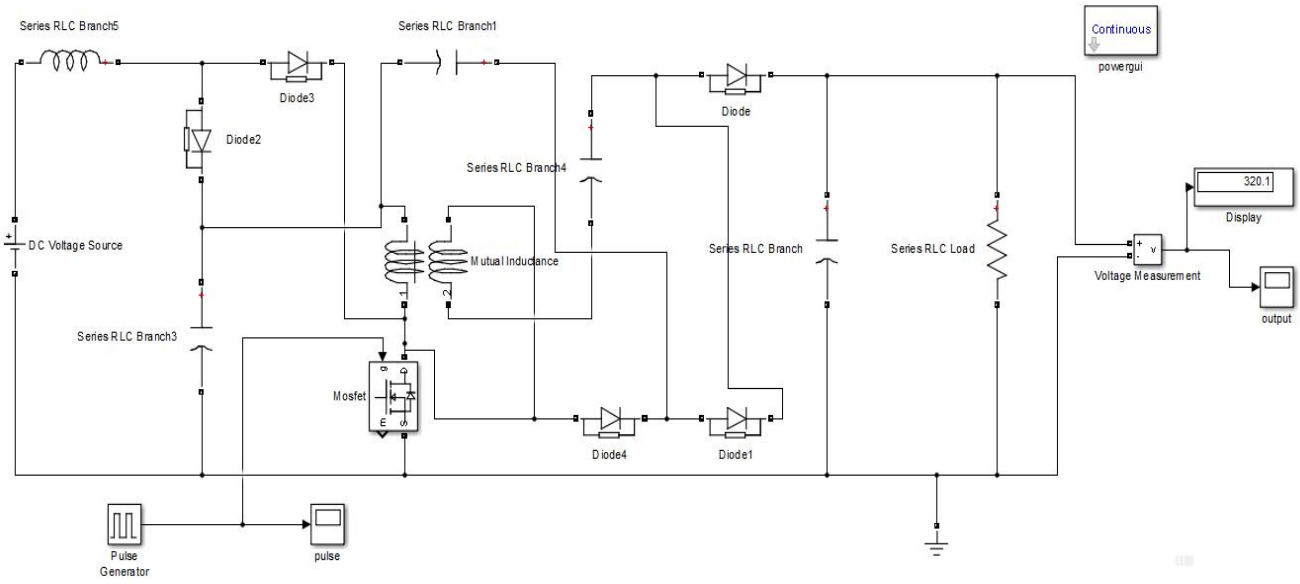

Fig. 6: MATLAB/SIMULINK Model of the converter

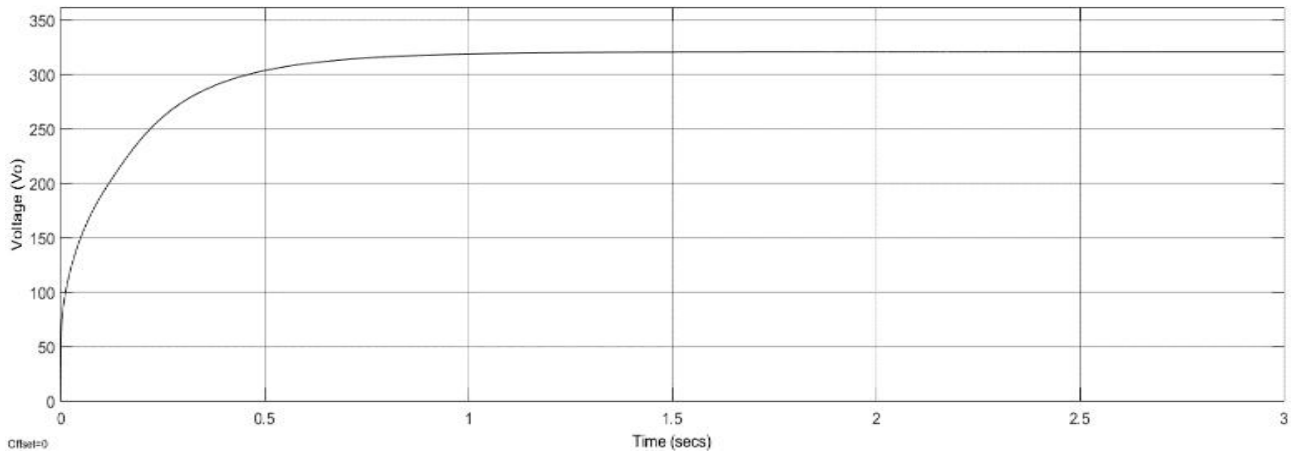

Fig. 7: Output Voltage

The results clearly indicate that the proposed converter is working properly, and the result waveform is very close to the theoretical values. From the Fig. 13 we can see that for the input voltage of 24 V the output is 320 V. so the gain of the converter is 13.33 from the simulation.

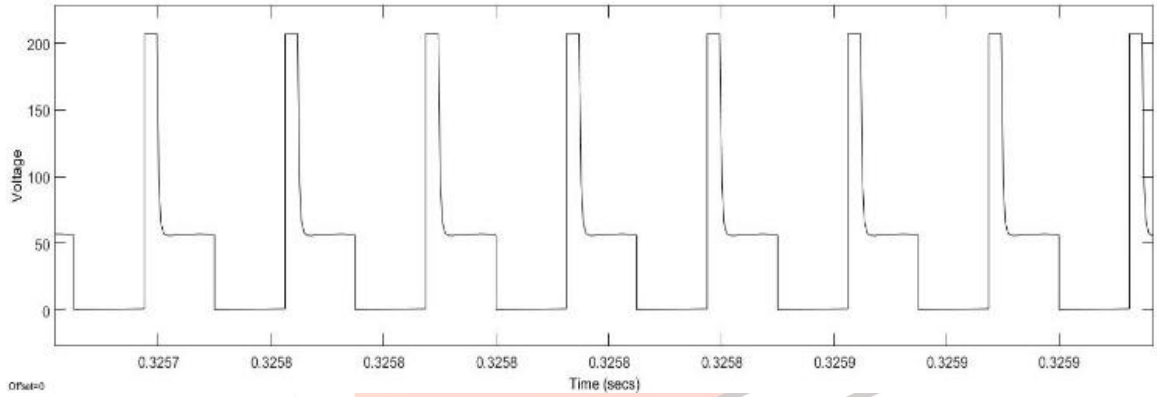

Fig. 8: Voltage stress across Switch Q (MOSFET)

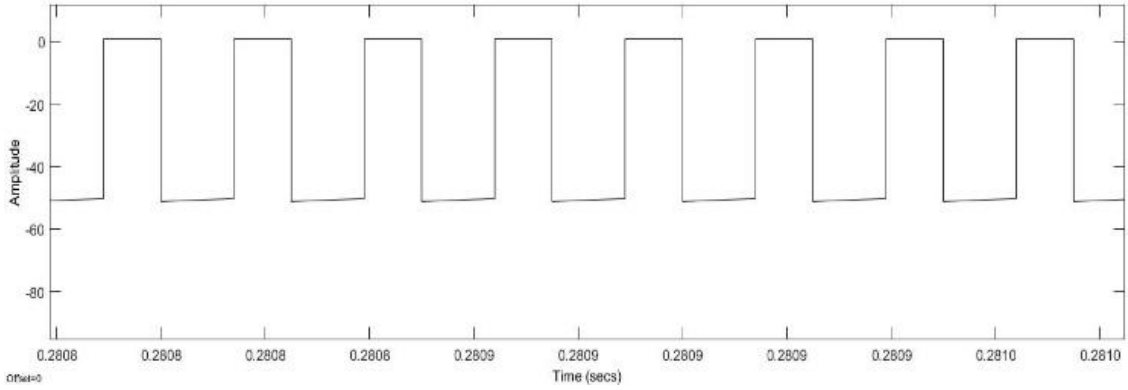

Fig. 9: Voltage stress across Diode-1

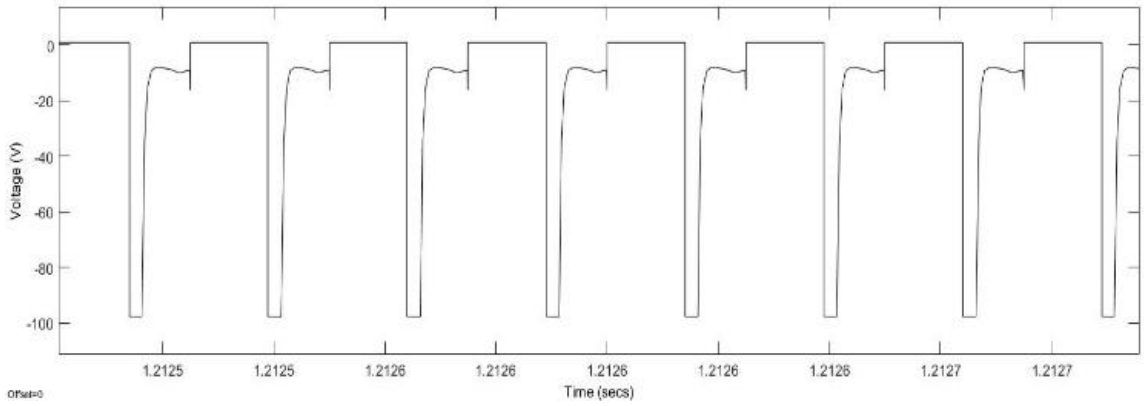

Fig. 10: Voltage stress across Diode-2

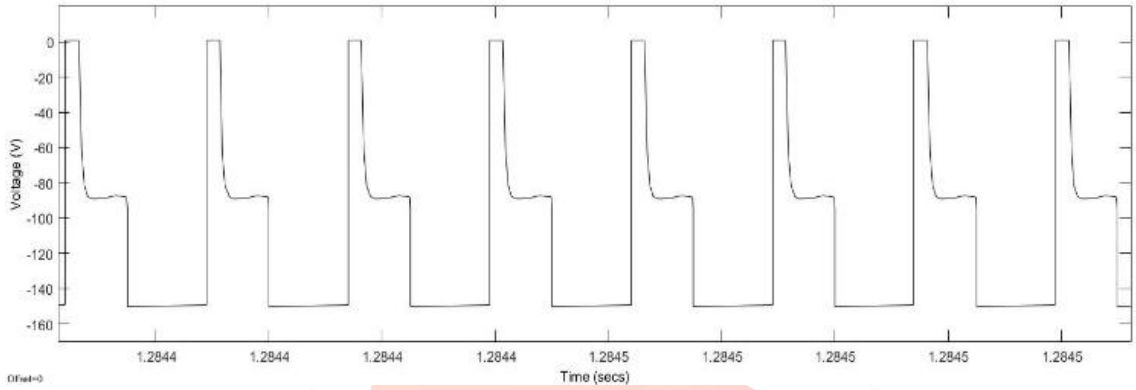

Fig. 11: Voltage stress across Diode-3

Fig.8 illustrates the voltage stress of Q. It can be seen that the voltage stress of the main switch is much lower level than output voltage when the main switch Q turns off. The voltage stress waveforms of the diodes D_1, D_2, and D_3 are demonstrated in Fig. 9 to Fig. 11. It is shown that the voltage stresses of these three diodes are far lower than the output voltage. From this we can say that lower voltage rating Switch and Diodes can be used. So for the switch the losses will be less and efficiency is improved.

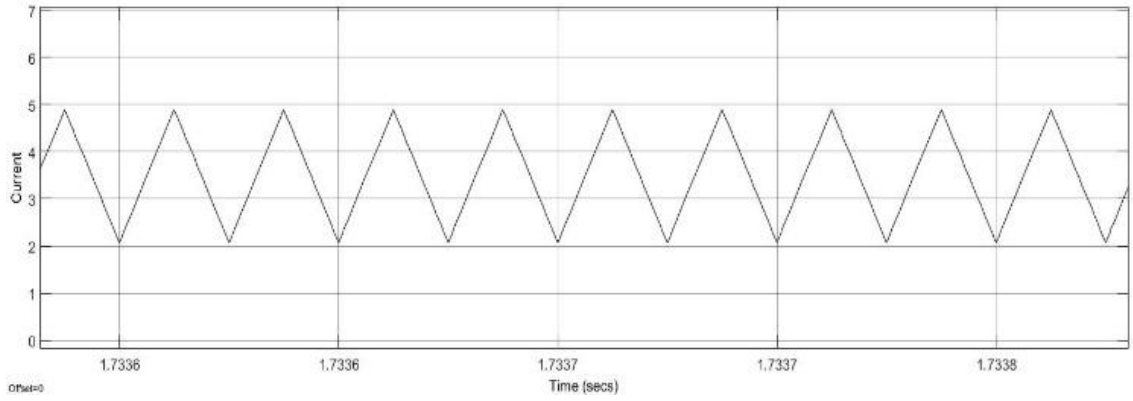

Fig. 12: Current waveform of i_{L1}

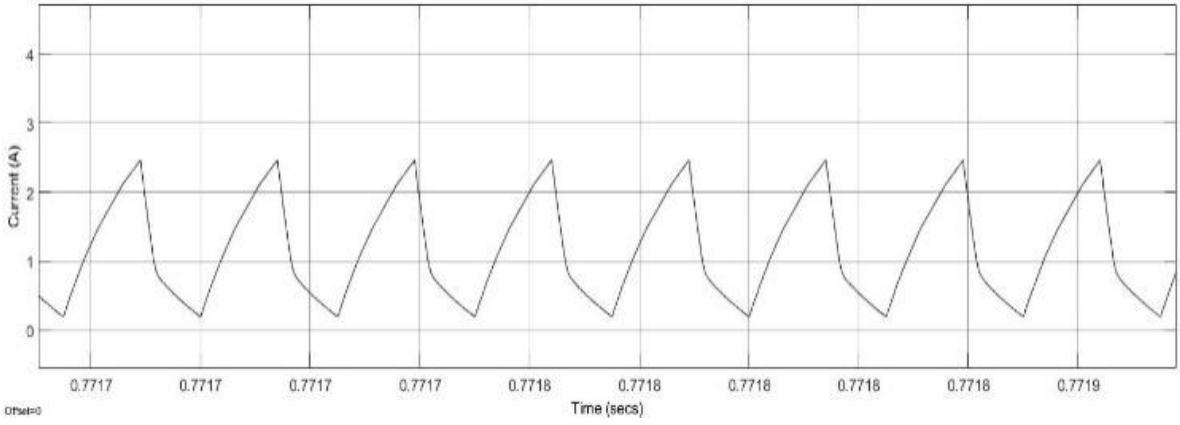

Fig. 13: Current waveform of i_{Lk1}

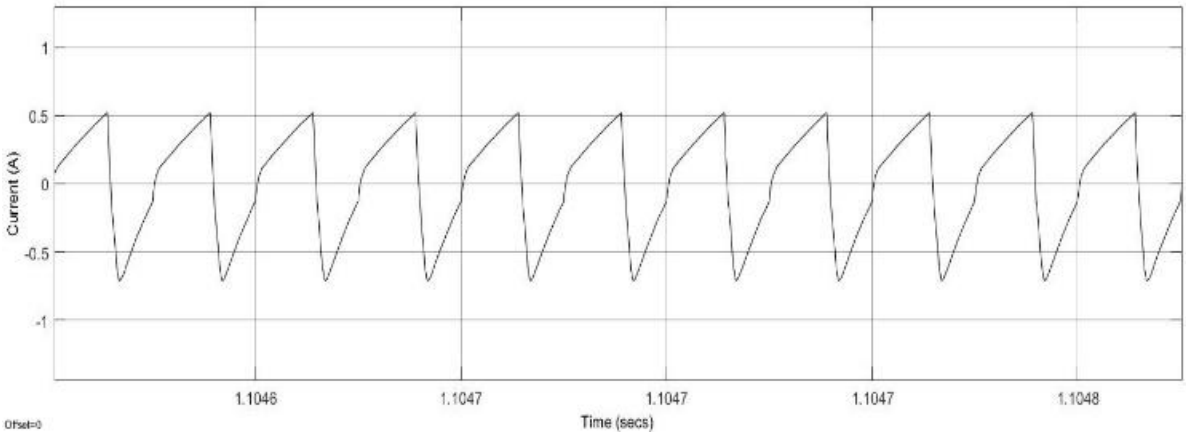

Fig. 14: Current waveform of i_{Lk2}

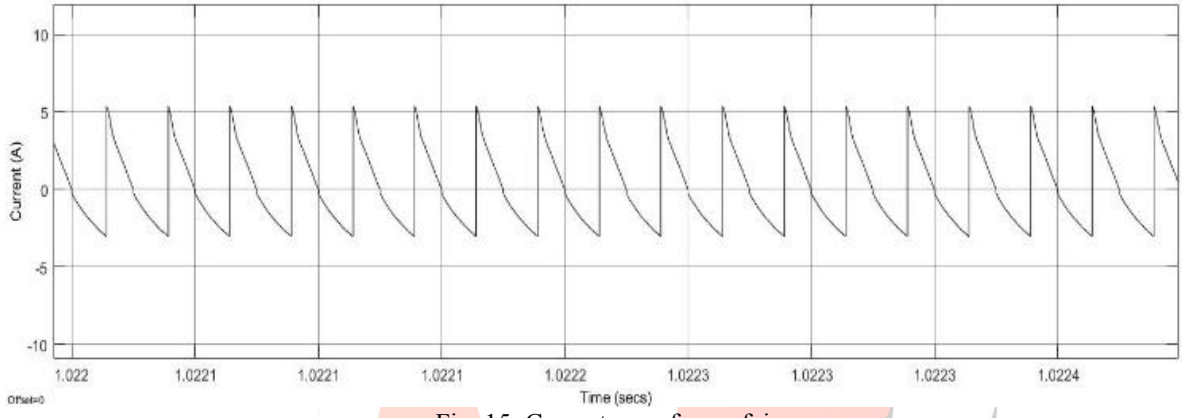

Fig. 15: Current waveform of i_{C1}

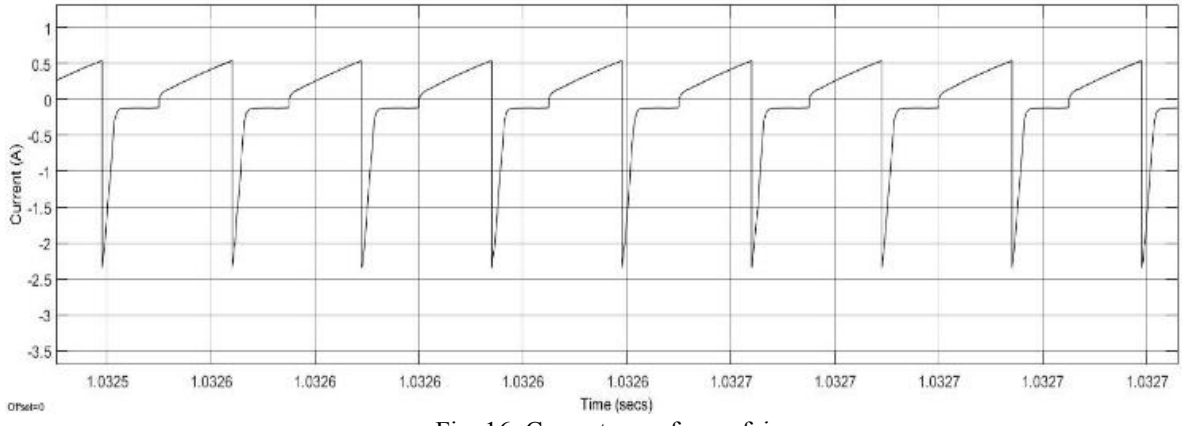

Fig. 16: Current waveform of i_{C2}

Fig. 12 to Fig. 14 shows the current waveforms including the input inductor current i_{L1}, the primary-side current i_{LK1} and the secondary-side current i_{LK2} of the coupled inductor. It can be seen that the input current is continuous, and this is optimal for the input current ripple cancellation, dynamic response improvement, and power device peak current reduction. Fig. 15 and Fig. 16 gives the measured current waveforms through C_1, and C_2, which can be verified through the theoretical analysis.

B. Proposed Converter Operating under Closed Loop System

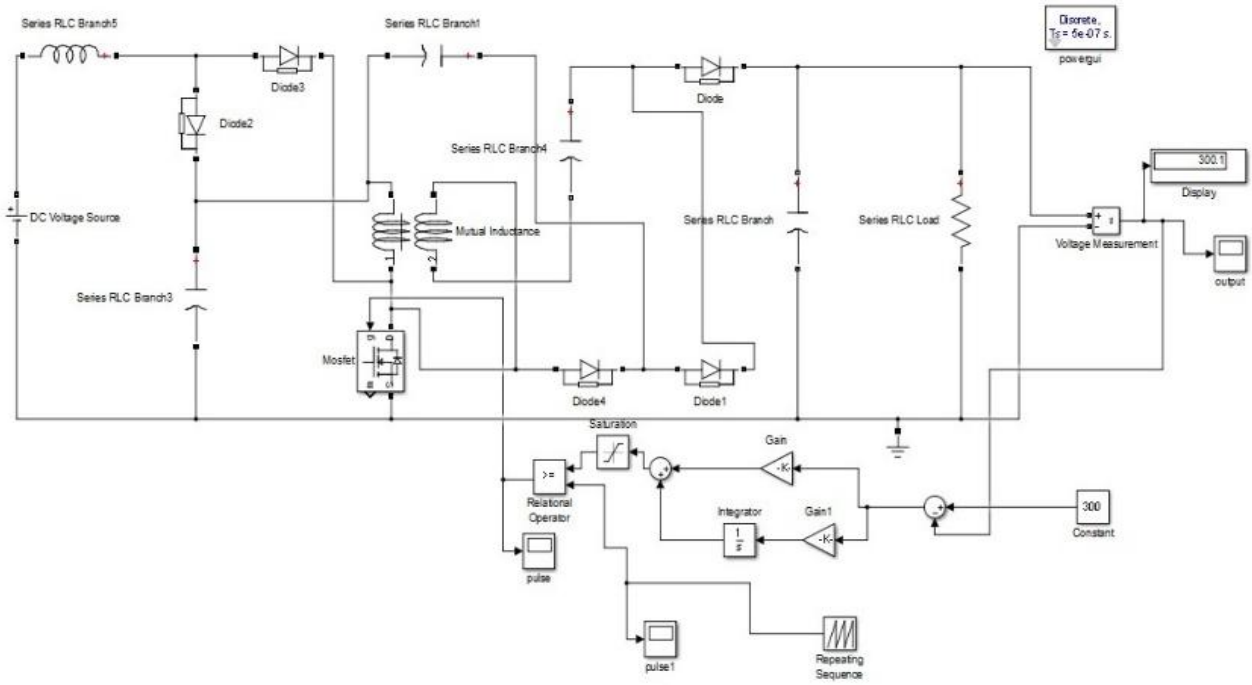

Fig. 17: MATLAB/SIMULINK Model of the closed loop system

As shown above in the simulation diagram, PI controller is used to control the output of the converter.

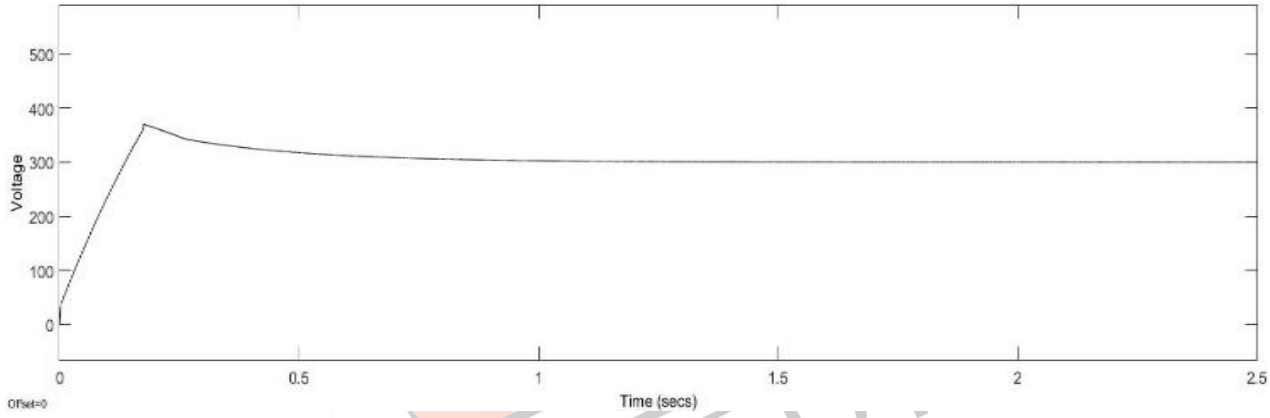

Fig. 18: Output voltage waveform when input is 24 volts (reference value 300V)

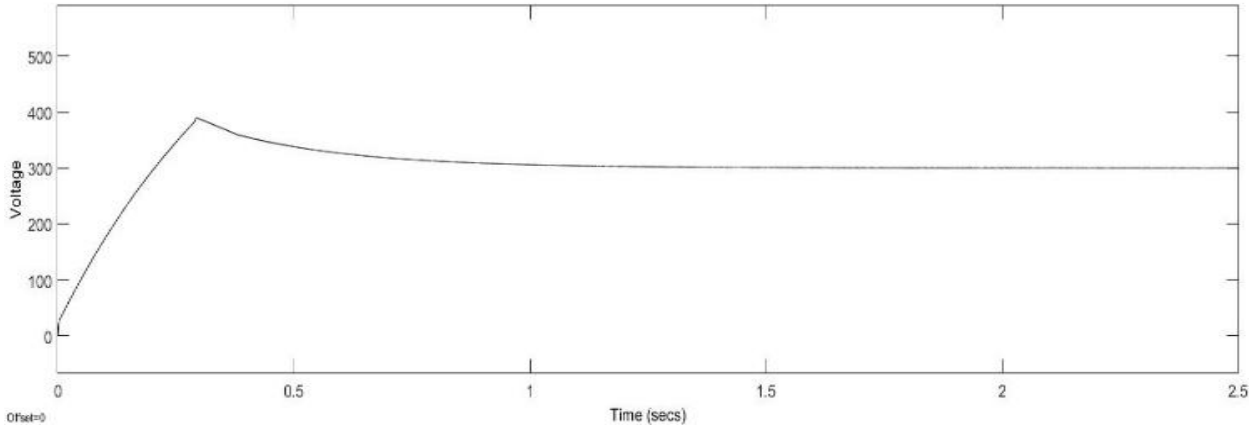

Fig. 19: Output voltage waveform when input is reduced to 18 volts (reference value 300V)

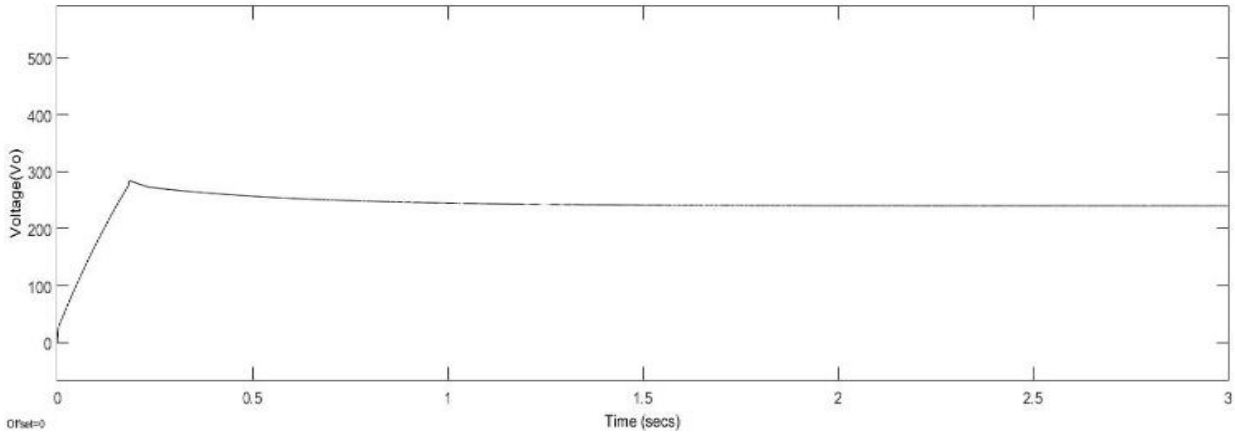

Fig. 20: Output voltage waveform when input is reduced to 18 volts (reference value 240V)

Form the above output waveforms we can say that, Because of the closed loop control, the output will be constant even if the PV-module is producing less amount of voltage.

Table 2 Summary

Sr. No.	Input (V)	Output (V)
Open Loop System		
1	24	320
2	18	240
Closed Loop System		
1	24	300 (reference value)
2	18	300 (reference value)
3	18	240 (reference value)

V. Conclusion

A High Gain DC-DC Boost Converter with Coupled Inductor for PV Systems with an active clamping circuit is introduced. From the simulation results it is shown that the gain of the converter is high. A clamped-capacitor circuit is connected to the primary side of the coupled inductor, the voltage stress of the active switch is reduced and the diode-capacitor in the secondary winding increases the voltage gain. In addition, the energy of secondary leakage inductor can be recycled and the turned off voltage spikes on the main switch are suppressed. Only one MOSFET is required to simplify the circuit configuration and improve the system reliability, and the proposed converter maintains the advantage of continuous input current. From the simulation results it is shown that the gain of the converter is high (≈13). Simulation verified the designs and calculations. The proposed PI controller effectively maintains the constant output voltage even if the input of the converter is changing. So, the problem of intermittent nature of PV terminal voltage can be mitigated using closed loop control and the objective of maintaining constant desired output voltage is achieved.

References

[1] A. E. Khosroshahi, L. Wang, H. Dadashzadeh, H. Ardi, A. Farakhor and A. M. Shotorbani, "A Two-Stage Coupled-Inductor-Based Cascaded DC-DC Converter with a High Voltage Gain," 2019 IEEE Canadian Conference of Electrical and Computer Engineering (CCECE), Edmonton, AB, Canada, 2019, pp. 1-5, doi: 10.1109/CCECE.2019.8861768.

[2] M. H. Rahman, S. K. Ghosh, M. S. Islam and A. K. Paul, "Design and Analysis of a High Efficiency Modified DC-DC Step Up Converter for PV System" 2019 IEEE International Conference on Power, Electrical, and Electronics and Industrial Applications (PEEIACON), Dhaka, Bangladesh, 2019, pp. 23-26, doi: 10.1109/PEEIACON48840.2019.9071949.

[3] M. sanwal, R. K. Singh and S. venkataramana, "High Gain DC-DC Converter using Coupled Inductors for Renewable Application," 2019 IEEE Students Conference on Engineering and Systems (SCES), Allahabad, India, 2019, pp. 1-5, doi: 10.1109/SCES46477.2019.8977224.

[4] A. S. Valarmathy and M. Prabhakar, "Coupled Inductor based High Gain DC-DC Converter for Renewable Energy Application," 2019 2nd International Conference on Power and Embedded Drive Control (ICPEDC), Chennai, India, 2019, pp. 516-521, doi: 10.1109/ICPEDC47771.2019.9036520

[5] M. Das and V. Agarwal, "Design and Analysis of a High-Efficiency DC–DC Converter With Soft Switching Capability for Renewable Energy Applications Requiring High Voltage Gain," in IEEE Transactions on Industrial Electronics, vol. 63, no. 5, pp. 2936-2944, May 2016, doi: 10.1109/TIE.2016.2515565.
[6] X. Hu and C. Gong, "A High Voltage Gain DC–DC Converter Integrating Coupled-Inductor and Diode–Capacitor Techniques," in IEEE Transactions on Power Electronics, vol. 29, no. 2, pp. 789-800, Feb. 2014, doi: 10.1109/TPEL.2013.2257870.
[7] M. L. Alghaythi, R. M. O'Connell, N. E. Islam and J. M. Guerrero, "Analysis and Design of a High Voltage Gain Interleaved DC-DC Converter with Dual Coupled Inductors and Voltage Multiplier Cell," 2020 IEEE Kansas Power and Energy Conference (KPEC), Manhattan, KS, USA, 2020, pp. 1-6, doi: 10.1109/KPEC47870.2020.9167671.
[8] M. B. da Rosa, M. Berrehil El Kattel, R. Mayer and S. V. Garcia Oliveira, "Experimental Results of a Bidirectional Coupled Inductor DC-DC Converter," 2019 IEEE 15th Brazilian Power Electronics Conference and 5th IEEE Southern Power Electronics Conference (COBEP/SPEC), Santos, Brazil, 2019, pp. 1-6, doi: 10.1109/COBEP/SPEC44138.2019.9065476.
[9] B. W. Williams, "DC-to-DC Converters With Continuous Input and Output Power," IEEE Trans. Power Electron., vol. 28, no. 5, pp. 2307–2316, May 2013.
[10] B.-M. Han, "Grid-tied power converter for battery energy storage composed of 2-stage DC-DC converter," in 2013 IEEE Power Energy Society General Meeting, 2013, pp. 1–5.
[11] Y. M. Chen, A. Q. Huang, and X. Yu, "A High Step-Up Three-Port DC-DC Converter for Stand-Alone PV/Battery Power Systems," IEEE Trans. Power Electron., vol. 28, no. 11, pp. 5049–5062, Nov. 2013.
[12] M. Jain, M. Daniele, and P. K. Jain, "A bidirectional DC-DC converter topology for low power application," IEEE Trans. Power Electron., vol. 15, no. 4, pp. 595–606, Jul. 2000.
[13] L. Roggia, L. Schuch, J. E. Baggio, C. Rech, and J. R. Pinheiro, "Integrated Full-Bridge-Forward DC-DC Converter for a Residential Microgrid Application," IEEE Trans. Power Electron., vol. 28, no. 4, pp. 1728–1740, Apr. 2013.
[14] R. T. Naayagi, A. J. Forsyth, and R. Shuttleworth, "High-Power Bidirectional DC-DC Converter for Aerospace Applications," IEEE Trans. Power Electron., vol. 27, no. 11, pp. 4366–4379, Nov. 2012.
[15] A. K. Rathore, D. R. Patil, and D. Srinivasan, "Non-isolated Bidirectional SoftSwitching Current-Fed LCL Resonant DC/DC Converter to Interface Energy Storage in DC Microgrid," IEEE Trans. Ind. Appl., vol. 52, no. 2, pp. 1711–1722, Mar. 2016.
[16] Wu, Tsai-Fu & Lai, YS & Hung, Jc & Chen, YM. (2005). Boost Converter with Coupled Inductors and Buck-Boost Type of Active Clamp. 399 - 405. 10.1109/PESC.2005.1581655.